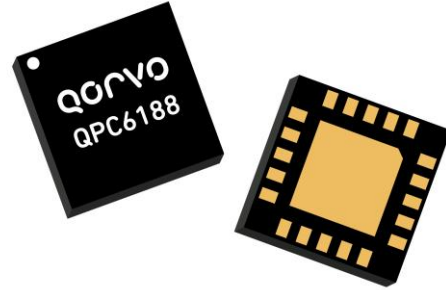


### 1. Product Overview and Benefits

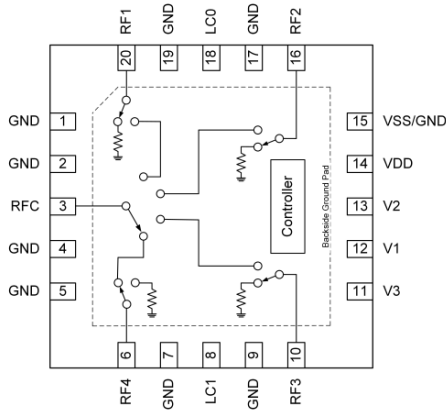
The Qorvo® QPC6188 is a Silicon on Insulator (SOI) Single-Pole 4- Throw (SP4T) switch designed for uses in cellular, 3G, LTE and other high-performance communication systems. It offers a high isolation, symmetric throw ports with excellent linearity and power handling capability. The design is non-reflective as such the RF1, RF2, RF3 and RF4 ports are terminated with 50 Ω load(s) in the non-throw or OFF state. QPC6188 is JEDEC standard 1.2V, 1.5V and 1.8V positive control logics selectable. It incorporates a single pin control to disable the internal Negative Voltage Generator (NVG) by applying a negative voltage of an off-chip external source to the same pin.

The QPC6188 is packaged in a RoHS-compliant, compact 3x3mm surface-mount leadless LGA package.



20 Pin 3 x 3 mm leadless SMT Package

### 2. Functional Block Diagram



Top View

### 3. Key Features

- 50MHz-8.6GHz Operational Frequency Range
- Symmetrical SP4T
- High Isolation: 50dB
- High Input IP3: +57dBm Typical
- Non-Reflective RF1, RF2 RF3, and RF4 Ports, Terminated in All-OFF State
- Ideal for DPD Feedback Path Selections and Calibration
- Only Requires a Single DC Supply with Internal NVG
- External Negative DC Supply Optional
- No Blocking Capacitors Required on RF Pins unless ≠0 DC Voltage Present
- 1.2V, 1.5V and 1.8V JEDEC Standard Control Logic Selectable

### 4. Applications

- Wireless Infrastructure
- High Performance Communication System
- Test Equipment

### 5. Ordering Information(TBD)

Part Number	Description
QPC6188SB	5pcs bag
QPC6188TR7	2500pcs on a 7" reel
QPC6188EVB	Evaluation Board

## 6. Electrical Characteristics

### 6.1. Absolute Maximum Ratings

Parameter	Conditions	Rating
Storage Temperature		-50°C to 150°C
VDD		+6V
Control Voltage		+6V
RF input power	ON state	+37dBm
	OFF state, internal termination	+23.5dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

### 6.2. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
VDD	+3.0	+5.0	+5.5	V
VSS	-5.5	-5.0	-3.0	V
RF Input Power, On State, CW			30	dBm
RFX Input Power, Off State, CW			23	dBm
Hot Switching RF Input Power, CW			23	dBm
T <sub>CASE</sub>	-40		+115	°C
T <sub>j</sub> for >10 <sup>5</sup> hours MTTF			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

### 6.3. Electrical Specifications

Parameter	Conditions <sup>(1)</sup>	Min.	Typ.	Max.	Units
Operating temperature range		-40°C		105°C	
Operable Temperature range		-40°C		115°C	
Operational Frequency Range		0.05		8.6	GHz
Test Frequency		0.05		8.6	GHz
Insertion Loss <sup>(2)</sup>	50-1000MHz		0.73	2	dB
	1000-3000MHz		0.85	2	dB
	3000-6000MHz		1.06	2	dB
	6000-8600MHz		1.19	2	dB
Insertion Loss Ripple	In any 600MHz range			0.5	dB
Insertion Loss Ripple	In any 800MHz range			0.8	dB
Return Loss, RFX (ON State)	50-1000MHz	15	25		dB
	1000-3000MHz	15	20		dB
	3000-6000MHz	15	15		dB
	6000-8600MHz	12	15		dB
Return Loss, RFC (ON State)	50-1000MHz	15	23		dB
	1000-3000MHz	15	20		dB
	3000-6000MHz	15	20		dB
	6000-8600MHz	12	15		dB



Parameter	Conditions <sup>(1)</sup>		Min.	Typ.	Max.	Units
Return Loss, RFX (OFF State)	50-1000MHz			23		dB
	1000-3000MHz			20		dB
	3000-5600MHz			20		dB
	6000-8600MHz			15		dB
Isolation RFC-RFX	50-1000MHz		45	63		dB
	1000-3000MHz		45	55		dB
	3000-6000MHz		45	52		dB
	6000-8600MHz		40	47		dB
Isolation RFX-RFX	50-1000MHz		35	62		dB
	1000-3000MHz		35	54		dB
	3000-6000MHz		35	52		dB
	6000-8600MHz		30	46		dB
IP3, +17dBm input power per-tone, 1MHz tone spacing	50-1000MHz		55	57		dBm
	1000-3000MHz		55	57		dBm
	2500MHz		55	57		dBm
	4000MHz		55	57		dBm
	3000-6000MHz		55	57		dBm
	6000-8600MHz		55	57		dBm
P0.1dB	50-1000MHz		30	39		dBm
	1000-3000MHz		30	39		dBm
	3000-5000MHz		30	39		dBm
	5000-8600MHz		30	39		dBm
VDD Current	VDD 3.0V to 5.5V			90	600	μA
Control Logic Voltage	1.2V Logic Low	JEDEC Standard Compatible	-0.30		0.46	V
	1.2V Logic High		0.72		VDD	V
	1.5V Logic Low		-0.30		0.56	V
	1.5V Logic High		0.91		VDD	V
	1.8V Logic Low		-0.30		0.68	V
	1.8V Logic High		1.07		VDD	V
Switching Time	Control Threshold to 90/10% RF, 2GHz			130	500	ns
	Control Threshold to 97% RF, 2GHz					ns
	Control Threshold to 99% RF, 2GHz			245	1000	ns
Settling Time	Control Threshold to 0.1dB Steady State Error				1000	ns
Thermal Resistance	Case to Termination			TBD		°C/W
	Case to RF Branch			TBD		°C/W

Notes:

1. Test conditions unless otherwise noted: VDD +3.0V, VSS 0V internal NVG enabled, Temp +25°C, RF ports DC potential 0V
2. PCB trace loss deducted

## 7. [Truth | Logic] Table

### 7.1. Switch Control Truth Table

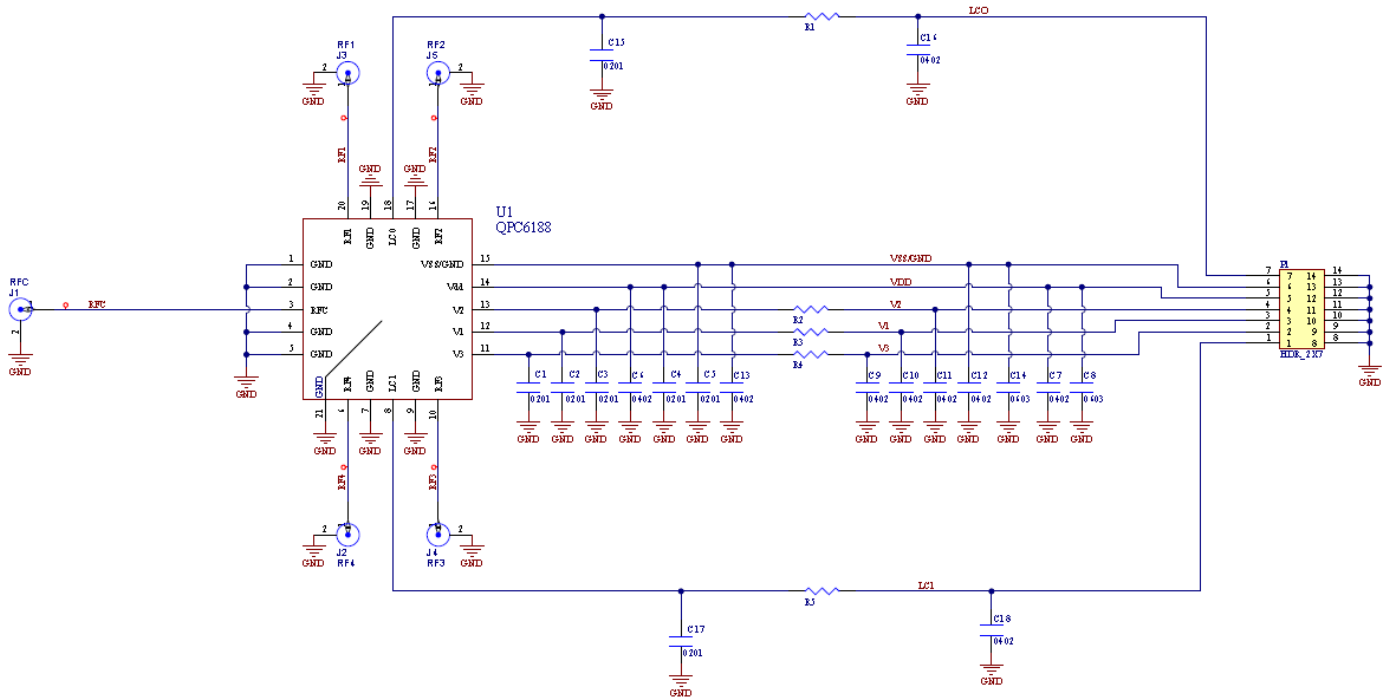
Control Input			Mode of Signal Path
V3	V2	V1	
0	0	0	RFC $\leftrightarrow$ RF1, Active ON
0	0	1	RFC $\leftrightarrow$ RF2, Active ON
0	1	0	RFC $\leftrightarrow$ RF3, Active ON
0	1	1	RFC $\leftrightarrow$ RF4, Active ON
1	X	X	All OFF

### 7.2. Control Logic Standard Selection Truth Table

Input		Control Logic Standard
LC1	LC0	
0	0	+1.5V
0	1	+1.8V
1	0	+1.2V
1	1	+1.8V

## 8. Application Information

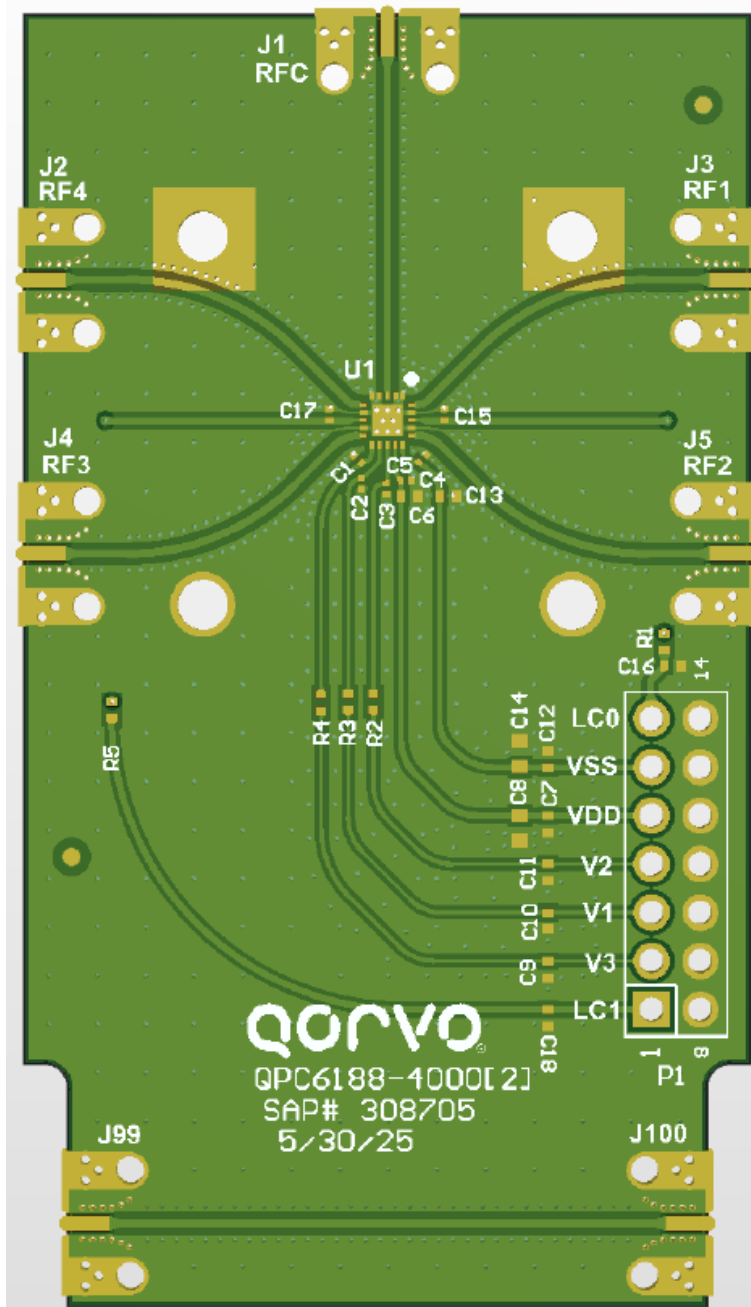
### 8.1. Application Circuit Schematic



### 8.2. Bill of Material

Ref. Des.	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board	-	-
U1	-	0.05-8.6GHz High Isolation SP4T Switch	Qorvo	QPC6188
C4, C5	100pF	CAP, 100pF,5%, 25V, COG, 0201	Kamaya	0201N101J250CT
C8, C13	0.1μF	CAP, 0.1μF, 10%, 50V, X7R, 0402	Various	-
R1, R2, R3, R4, R5	0 Ω	RES, 0 OHM, 5%, 1/20W, 0201	Kamaya	RMC1/20JPPA
J1, J2, J3, J4, J5	SMA	CON, SMA, EL FLT VIPER MAT-21-1038	Amphenol	901-10425
P1	-	CON, HDR, 2x7 RT-ANG, 0.100", T/H	SAMTEC	TSW-107-08-G-D-RA

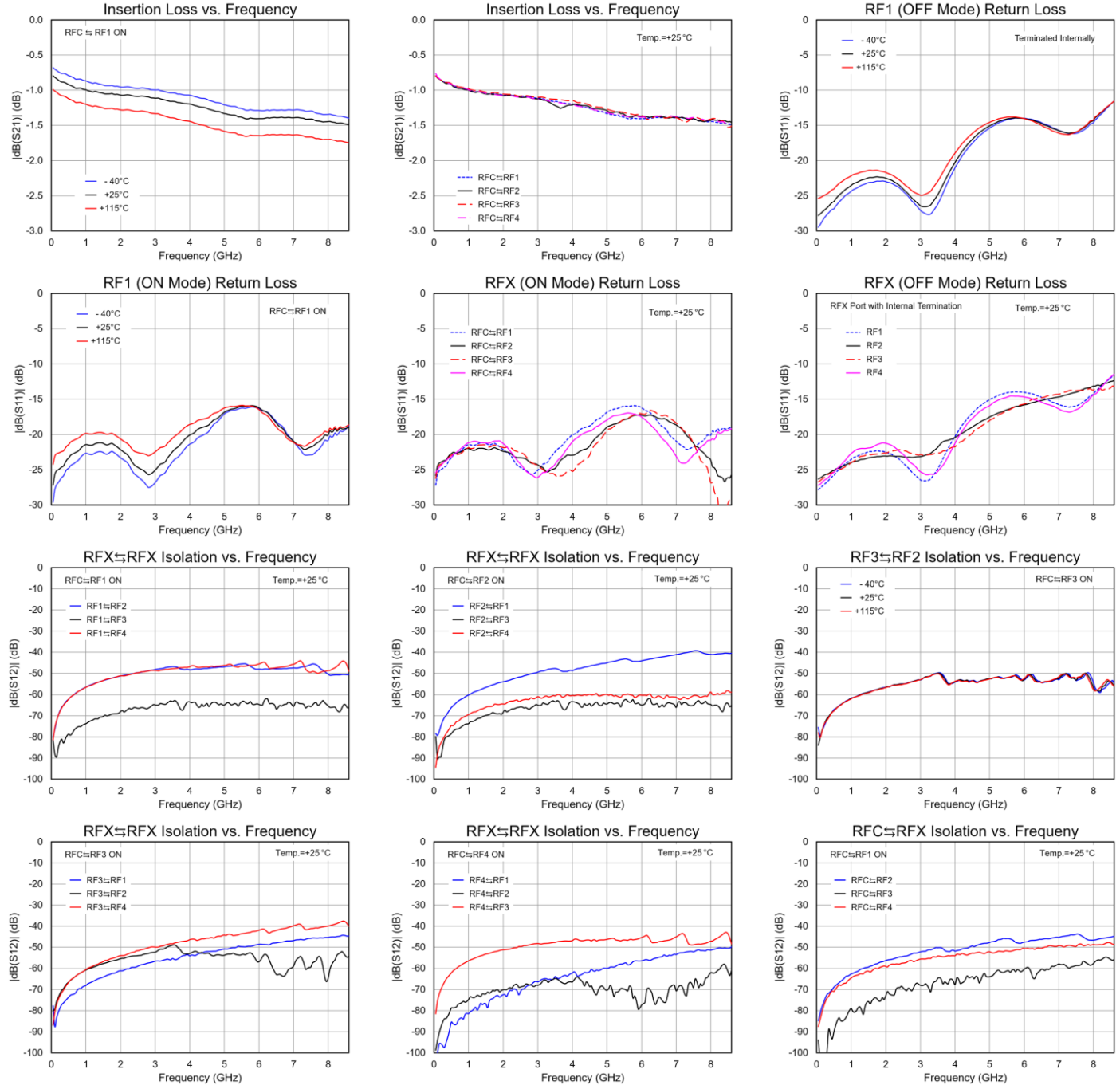
#### 8.3. Application PCB Layout



EVB Layout Top View

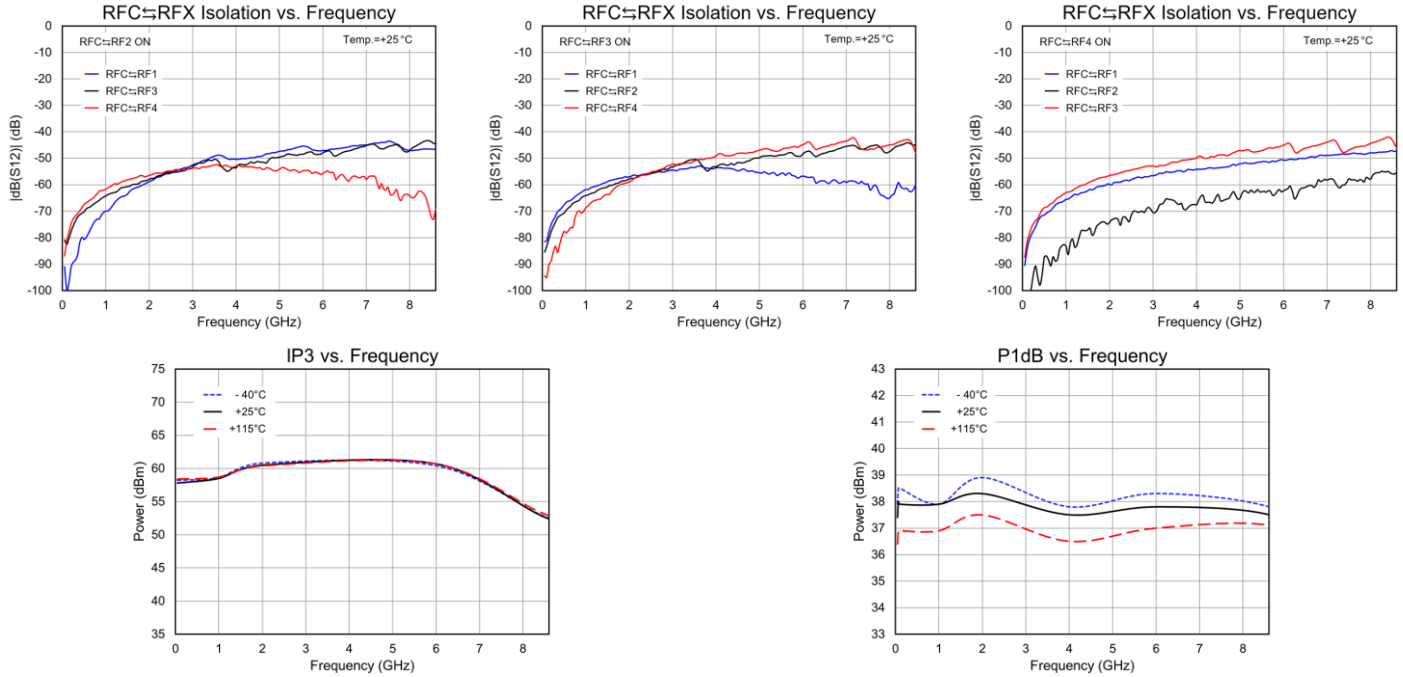
## 9. Performance Plots

Test conditions unless otherwise noted: VDD +3.3V, Reference on device pads, System impedance 50Ω, Temp +25°C

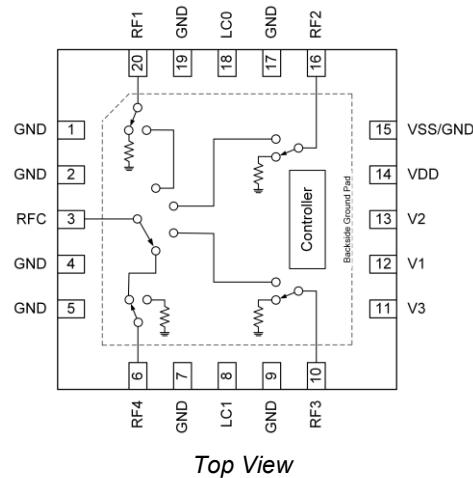


## 10. Performance plots (Continued 1)

Test conditions unless otherwise noted: VDD +3.3V, Reference on device pads, System impedance 50Ω, Temp +25°C



## 11. Pin Configuration and Description

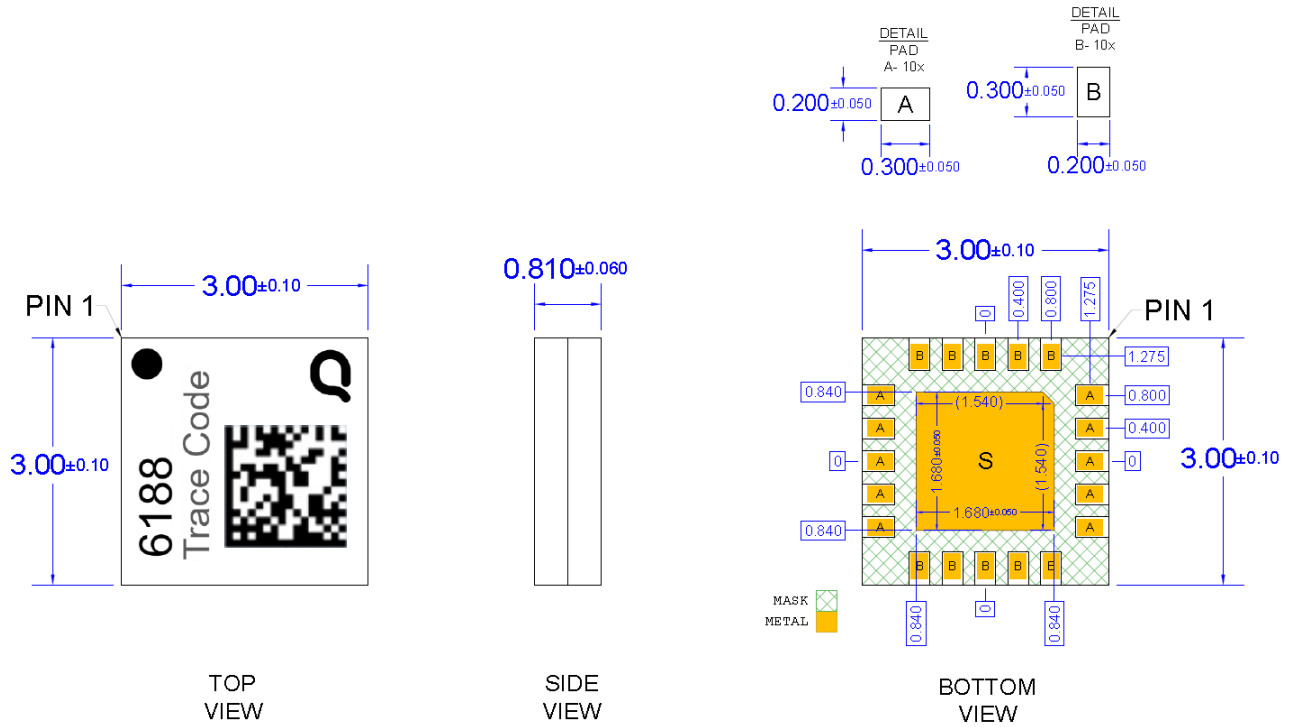


PIN NUMBER	LABEL	DESCRIPTION
1, 2, 4, 5, 7, 9, 17, 19	GND	Ground. No connection internally, can be left floating
3	RFC	RF input, internal 50Ω matched, DC potential 0V
6	RF4	RF output 4, internal 50Ω matched, DC potential 0V
8	LC1	Control Logic select input Pin 1
10	RF3	RF output 3, internal 50Ω matched, DC potential 0V
11	V3	Switch Control Logic input pin 3
12	V1	Switch Control Logic input pin 1
13	V2	Switch Control Logic input pin 2
14	VDD	Positive DC Voltage supply input
15	VSS	Negative DC Voltage supply or Selection input
16	RF2	RF output 2, internal 50Ω matched, DC potential 0V
18	LC0	Control Logic select input Pin 0
20	RF1	RF output 1, internal 50Ω matched, DC potential 0V
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB via holes under the device are required.

### 12. Packaging and Ordering Information

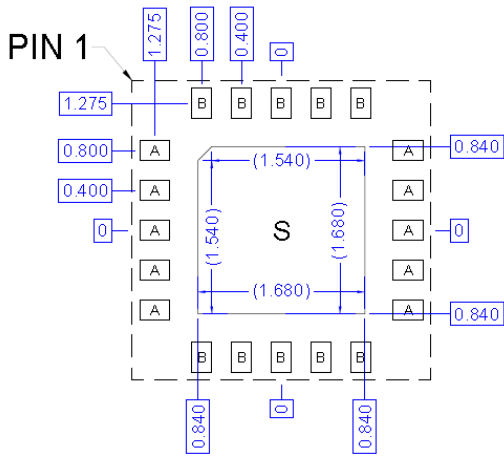
#### 12.1. Device Marking and Package Dimensions

Marking: Part number – QPC6188  
Trace code – assigned by Sub-contractor

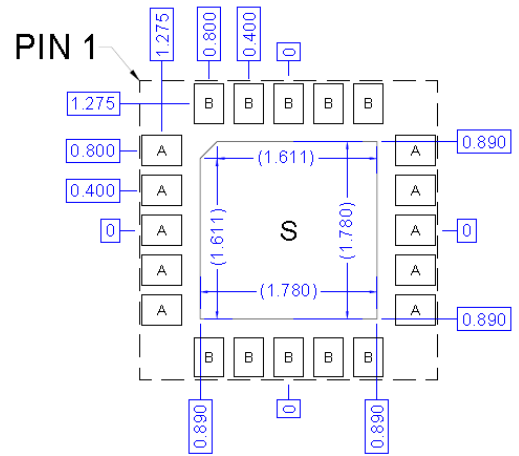


- Notes:
1. All dimensions are in mm. Angles are in degrees.
  2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
  3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

### 12.2. PCB Footprint Recommendations

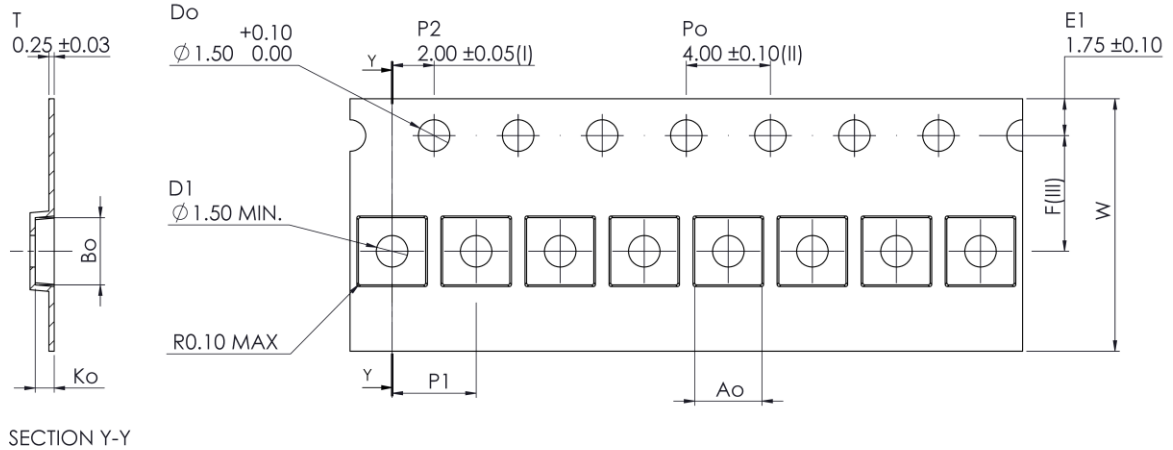


RECOMMENDED  
LAND PATTERN

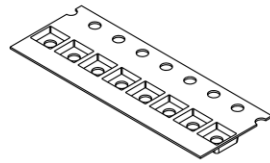


RECOMMENDED  
LAND PATTERN MASK

#### 12.3. Tape and Reel Information



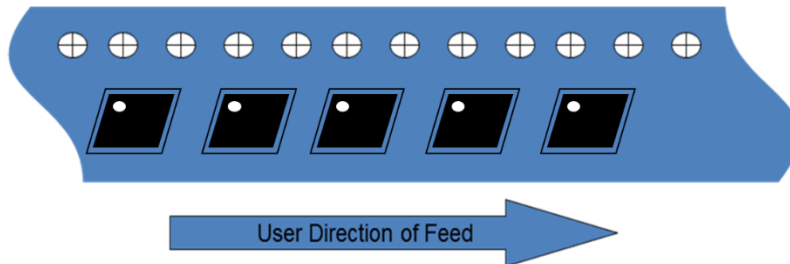
Ao	3.20	+/- 0.05
Bo	3.20	+/- 0.05
Ko	1.00	+/- 0.05
F	5.50	+/- 0.05
P1	4.00	+/- 0.10
W	12.00	+0.30/- 0.10



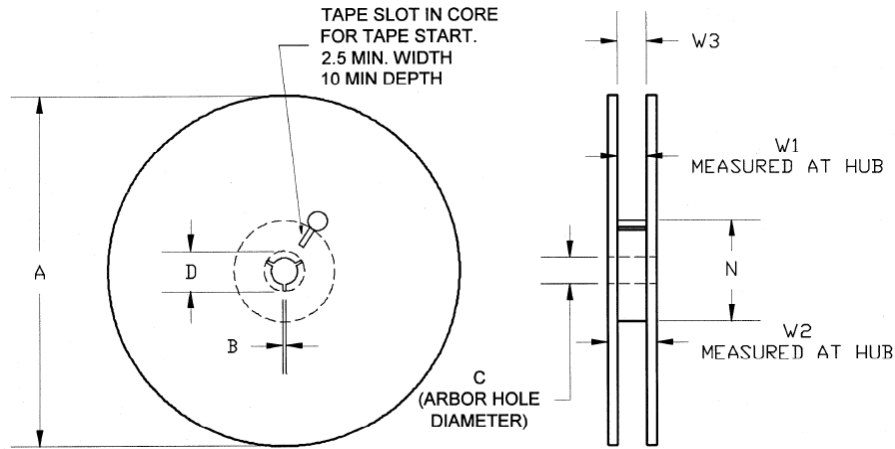
- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

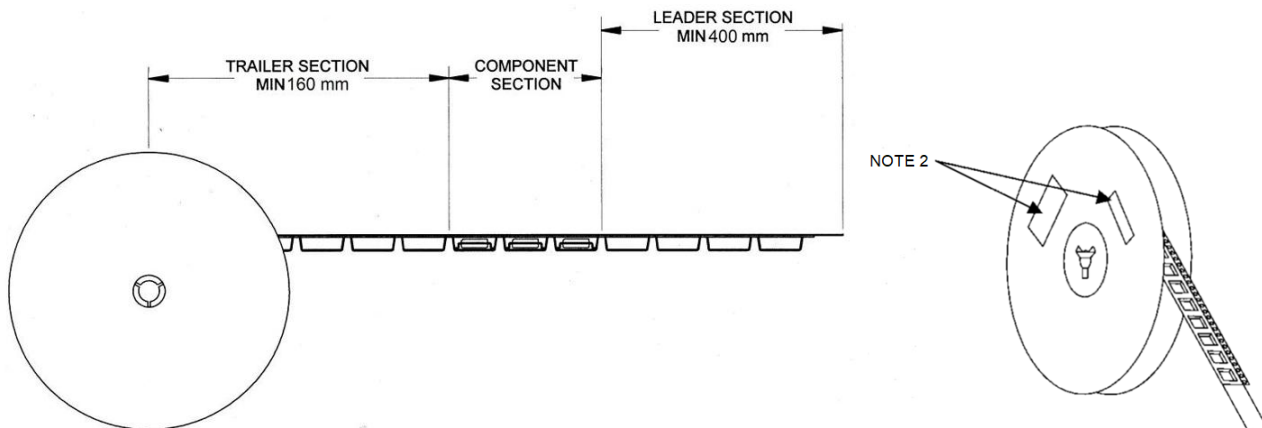
Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.125	3.20
	Width	B0	0.125	3.20
	Depth	K0	0.040	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width (Reference Only)	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.00



Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

### 13. Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020


**Caution!**

ESD sensitive device

### 14. Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Thin Ni-ENEPIG (*Plating thickness: Ni 0.40±0.10µm, Pd 0.145±0.035µm, Au 0.095±0.025µm*)

### 15. Environmental Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- SVHC Free
- PFOS Free





## Contact Information

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For the latest specifications, additional product information, worldwide sales and distribution locations:

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**Tel:** +1 844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

## Important Notices

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