

Product Overview

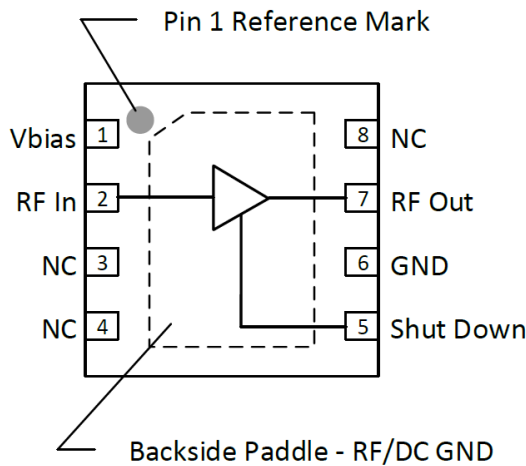
The QPL9058 is a high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. At 3.6 GHz, the amplifier typically provides 18 dB gain, +36 dBm OIP3 at a 54mA bias setting, and 0.6 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

The QPL9058 is bias adjustable and requires minimal external components to operate. It also has a power down control capability integrated into the die for TDD applications.



8 Pin 2X2 mm DFN Package

Functional Block Diagram



Top View

Key Features

- 0.5~6.0GHz Operational Bandwidth
- Low noise figure, 0.6dB NF at 3.6GHz
- 36dBm OIP3
- 18dB small signal gain
- Bias adjustable for linearity optimization
- Unconditionally stable
- Shut-down control with 1.8V logic
- Maintains OFF state with high Pin drive

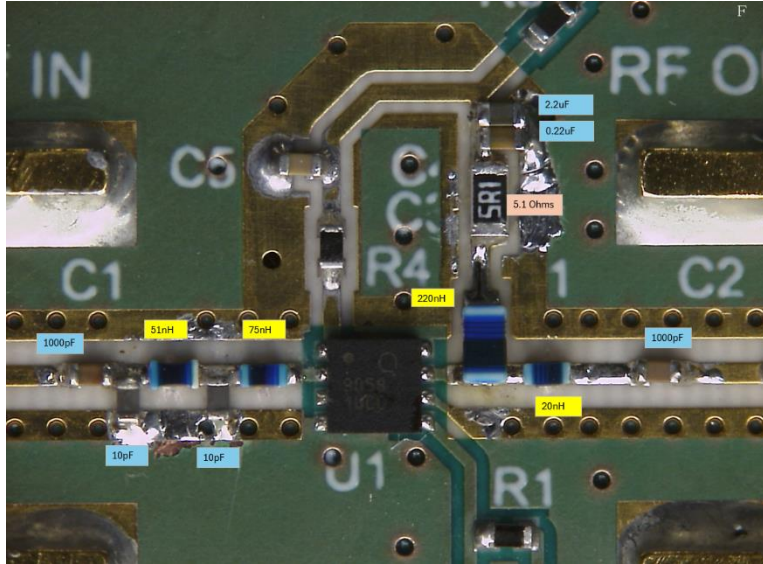
Applications

- 5G m-MIMO
- Repeaters / DAS
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

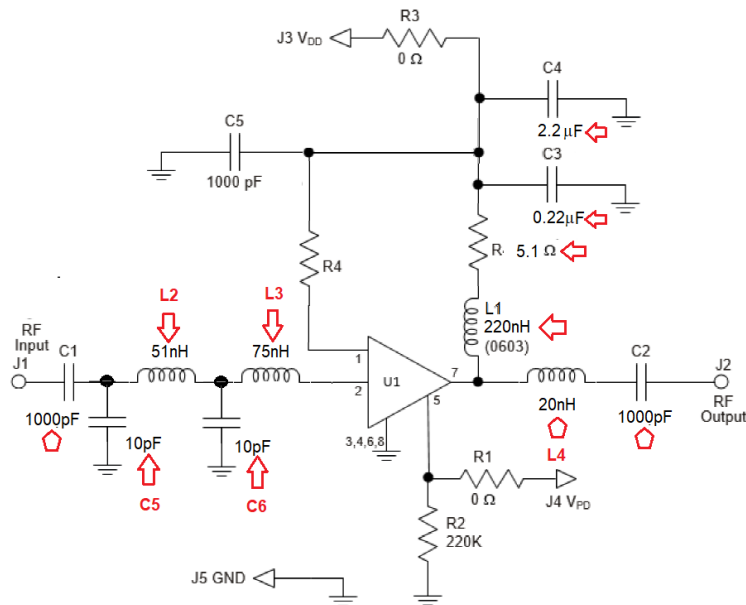
Part No.	Description
QPL9058TR7	2500 pieces on a 7" reel
QPL9058EVB-01	0.5-6.0 GHz Evaluation Board

174~216MHz Reference Board with on board Matchings



Notes:

1. C5 right edge to U1 left edge – 3.9mm
2. C6 right edge to U1 left edge – 2.0mm
3. L2 center to U1 left edge – 3.2mm
4. L3 center to U1 left edge – 1.3mm
5. L4 center to U1 right edge – 2.6mm



Notes:

1. For TDD Applications: R1 = 0Ω and R2 = 220K.
2. For FDD Applications: R2 = 220K 'OR' Pin 5 tied to ground. R1 = DNP/Omitted

Bill of Material – QPL9058 Reference Board of 174~216MHz

Reference Des.	Value	Description	Manuf.	Part Number
N/A	--	Printed Circuit Board	Qorvo	
U1	--	Ultra Low Noise QPL9058 LNA	Qorvo	QPL9058
R1, R3	0Ω	RES, 0Ω, 1/10W, 0402	various	
R2	220KΩ	RES, 220KΩ, 5%, 1/16W, 0402	various	
R4	3.83KΩ	RES, 3.83KΩ, 1%, 1/16W, 0402	various	
R	5.1Ω	RES, 5.1Ω, 0603	various	
C1, C2	1000pF	CAP, 1000pF, 10%, 50V, X7R, 0402	Murata	GRM155R71H102KA01D
C3	0.22μF	CAP, 0.22μF, 10%, X5R, 0402	various	
C4	2.21μF	CAP, 2.2μF, 10%, X5R, 0402	various	
C5, C6	10pF	CAP, 10pF, Hi-Q, 0402		
L1	220nH	IND, 220nH, 5%, W/W, 0603	Coilcraft	
L2	51nH	IND, 51nH, W/W, 0402		
L3	75nH	IND, 75nH, W/W, 0402		

Reference Board Performance – 174~216MHz

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 54\text{ mA}$ (typ.), Temp = +25°C

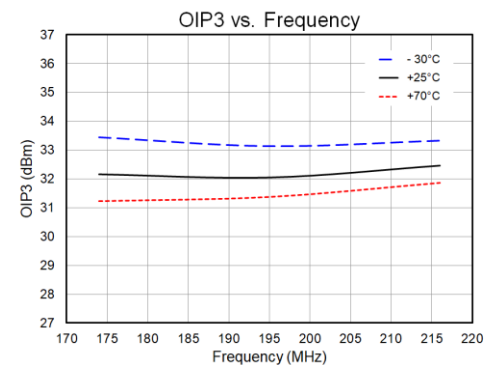
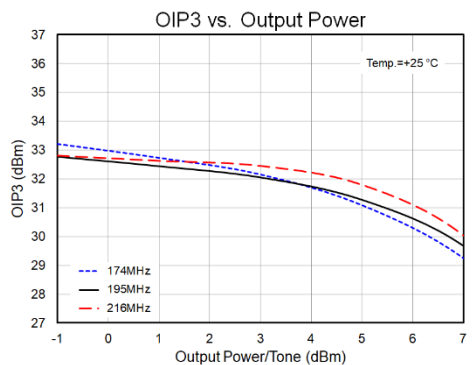
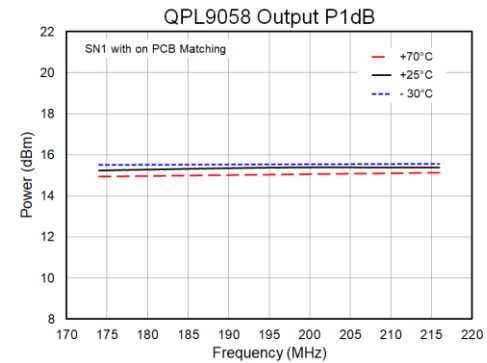
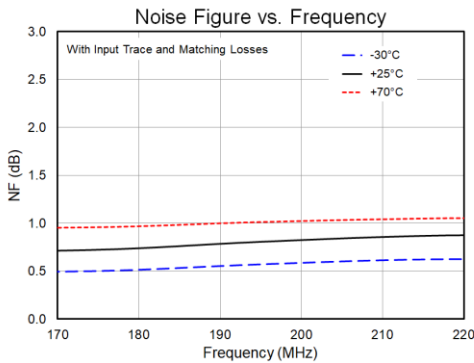
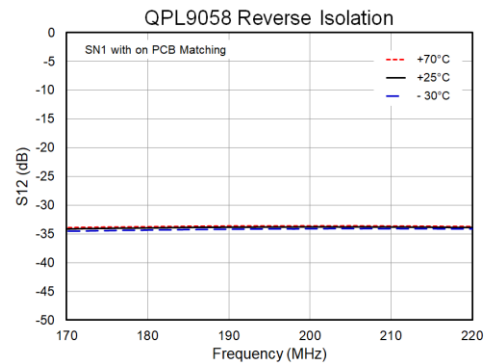
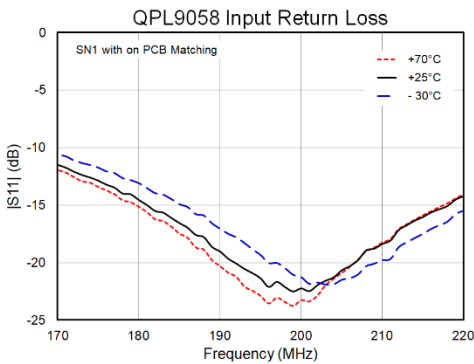
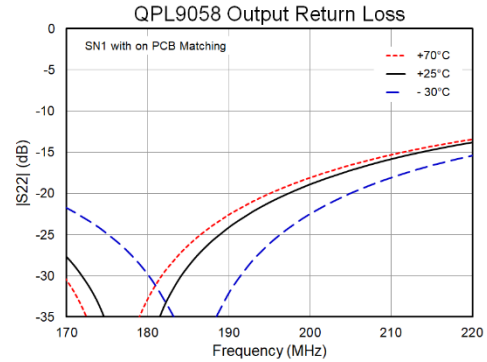
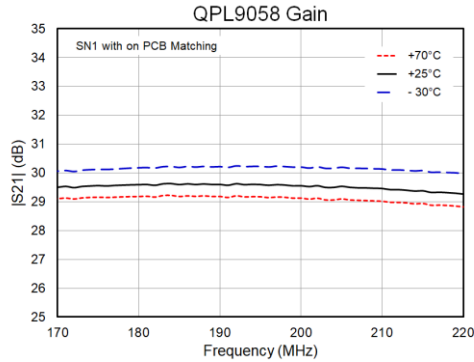
Parameter	Conditions	Typical Values			Units
Frequency		174	195	216	MHz
Gain		29.7	29.9	29.6	dB
Input Return Loss		12.6	21.4	15.6	dB
Output Return Loss		33.0	21.1	14.5	dB
Output P1dB		15.2	15.5	15.3	dBm
OIP3	$P_{out}=+2\text{ dBm/ tone, } \Delta f=1\text{ MHz}$	32.2	32.4	32.5	dBm
Noise figure ⁽¹⁾		0.72	0.80	0.87	dB

Note:

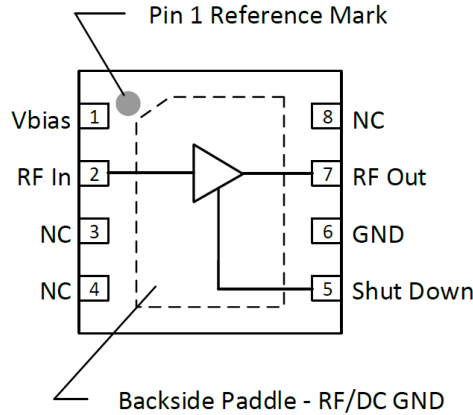
1. With Input trace and matching losses

Performance Plots – 174~216MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 54\text{ mA}$, $50\ \Omega$ system



Pad Configuration and Description

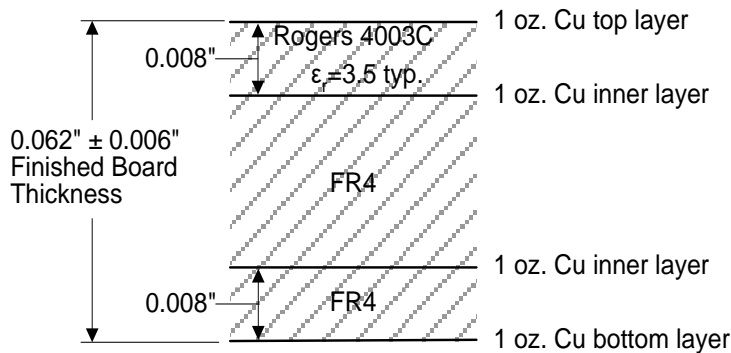


Top View

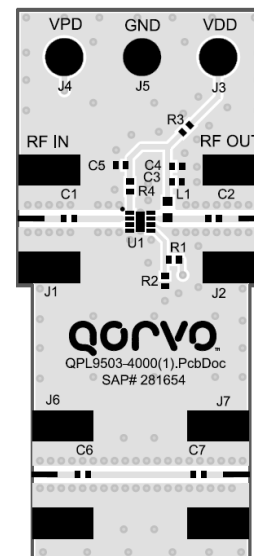
Pad No.	Label	Description
1	V _{bias}	Sets the LNA bias current for the device.
2	RF In	RF Input pin, internally matched to 50 ohms. A DC block is required.
5	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out	RF Output pin, internally matched to 50 ohms. A DC block is required. V _{DD} supply pin.
3, 4, 6, 8	NC	Not connected internally. This pin may be left floating or connected to ground.
Backside Paddle	RF/DC GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are recommended.

Evaluation Board PCB Information

Qorvo PCB Material and Stack-up



50 ohm line dimensions: width = 0.0182", spacing = 0.020"



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020E



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu (*Thickness: Ni 0.508 ~1.524 μm; Pd 0.023 ~ 0.1016 μm; Au 0.00254 ~ 0.01016 μm*)

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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