

Product Overview

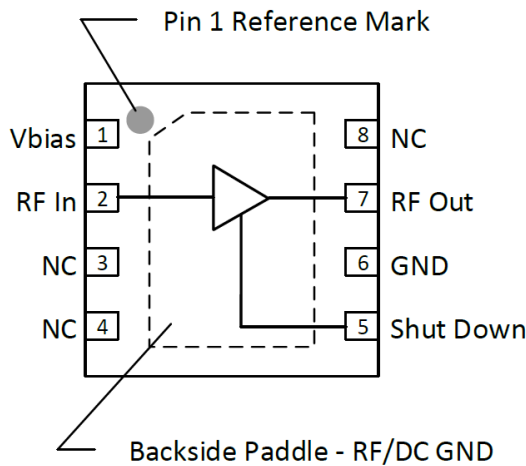
The QPL9058 is a high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. At 3.6 GHz, the amplifier typically provides 18 dB gain, +36 dBm OIP3 at a 54mA bias setting, and 0.6 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

The QPL9058 is bias adjustable and requires minimal external components to operate. It also has a power down control capability integrated into the die for TDD applications.



8 Pin 2X2 mm DFN Package

Functional Block Diagram



Top View

Key Features

- 0.5~6.0GHz Operational Bandwidth
- Low noise figure, 0.6dB NF at 3.6GHz
- 36dBm OIP3
- 18dB small signal gain
- Bias adjustable for linearity optimization
- Unconditionally stable
- Shut-down control with 1.8V logic
- Maintains OFF state with high Pin drive

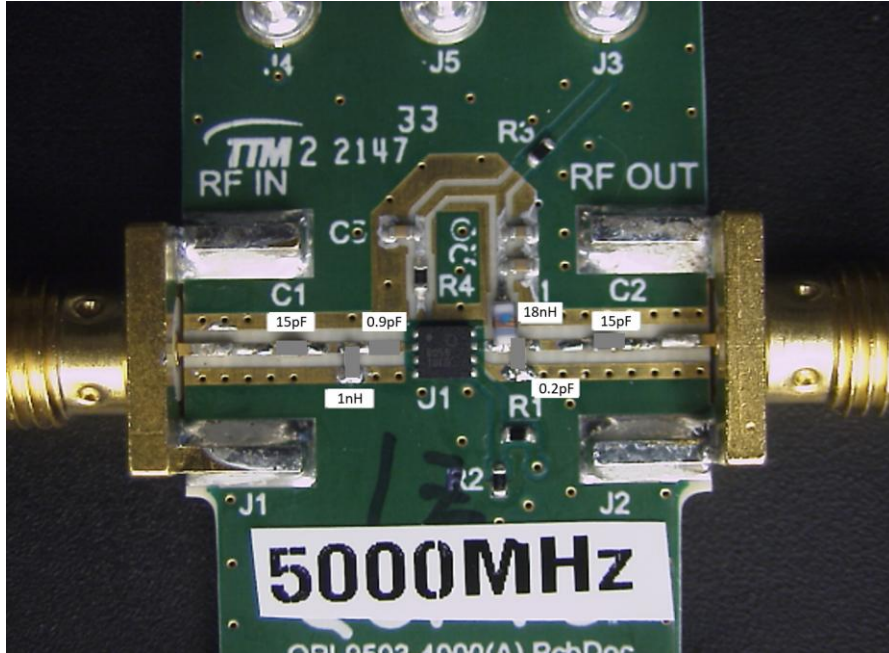
Applications

- 5G m-MIMO
- Repeaters / DAS
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

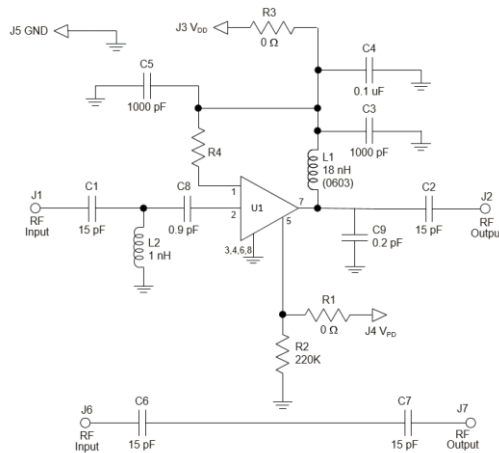
Part No.	Description
QPL9058TR7	2500 pieces on a 7" reel
QPL9058EVB-01	0.5-6.0 GHz Evaluation Board

4400~5000MHz Reference Board with on board Matchings



Notes:

1. Distance from right edge of C8 to left edge of U1 is 10mils.
2. Distance from left edge of L2 to right edge of U1 is 75 mils.
3. Distance from left edge of C9 to right edge of U1 is 165 mils.
4. R4 = 3.83KOhm



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size unless otherwise mentioned.
3. For TDD Applications: R1 = 0Ω and R2 = 220K.
4. For FDD Applications: R2 = 220K 'OR' Pin 5 tied to ground. R1 = DNP/Omitted
5. A through line is included on the evaluation board to deduct the board trace losses.
6. R4 sets the Idq current. Can be changed for the desired quiescent current.

Bill of Material – QPL9058 Reference Board of 4400~5000MHz

Reference Des.	Value	Description	Manuf.	Part Number
N/A	--	Printed Circuit Board	Qorvo	
U1	--	Ultra Low Noise QPL9058 LNA	Qorvo	QPL9058
R1, R3	0Ω	RES, 0Ω, 1/10W, 0402	various	
R2	220KΩ	RES, 220KΩ, 5%, 1/16W, 0402	various	
R4	3.83KΩ	RES, 3.83KΩ, 1%, 1/16W, 0402	various	
C1, C2, C6, C7	15pF	CAP, 15pF, 2%, 50V, Hi-Q, 0402	Murata	GJM1555C1H150JB01D
C3, C5	1000pF	CAP, 1000pF, 10%, 50V, X7R, 0402	Murata	GRM155R71H102KA01D
C4	0.1μF	CAP, 0.1μF, 10%, 50V, X5R, 0402	Various	
C8	0.9pF	CAP, 0.9pF, Hi-Q, 0402	Various	
C9	0.2pF	CAP, 0.2pF, Hi-Q, 0402	Various	
L1	18nH	IND, 18nH, 5%, 0603	Coilcraft	0603CS-18NXJL
L2	1nH	IND, 1nH, 5%, 0402	Various	

Reference Board Performance – 4400~5000MHz

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 54\text{ mA}$ (typ.), Temp = +25°C

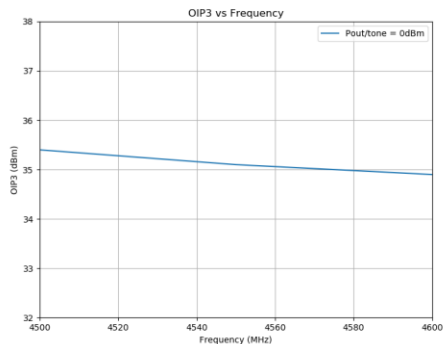
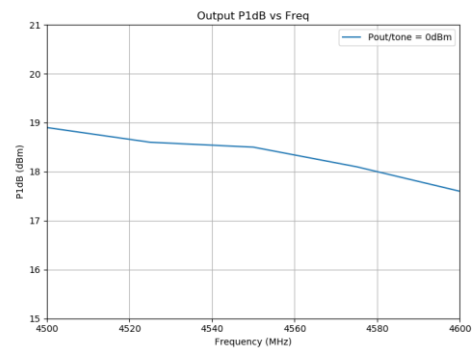
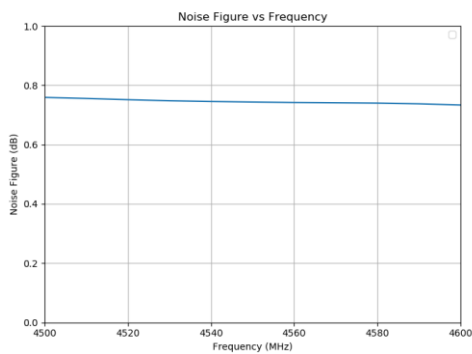
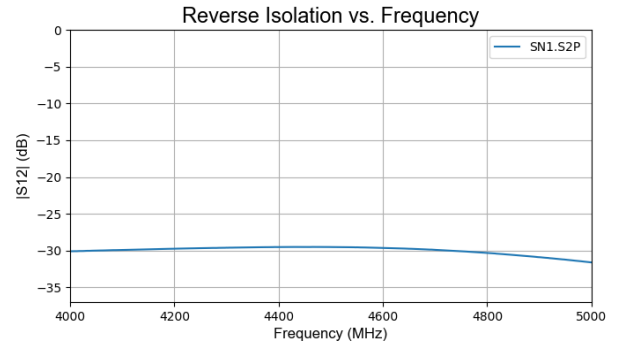
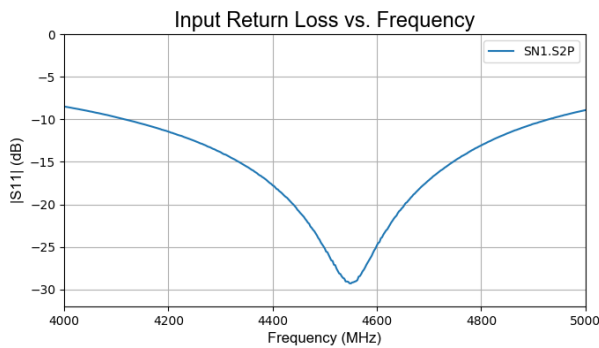
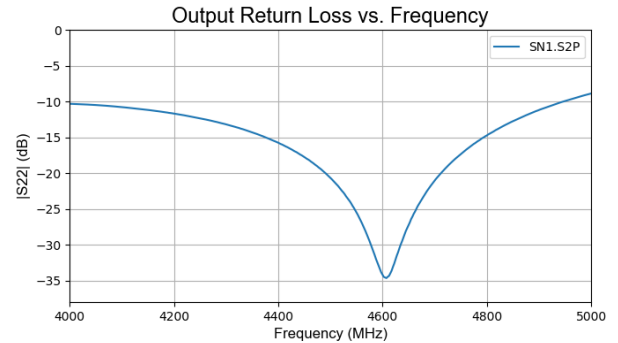
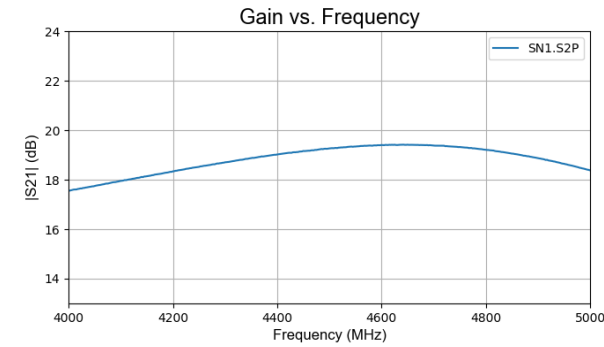
Parameter	Conditions	Typical Values				Units
Frequency		4500	4550	4575	4600	MHz
Gain		19.3	19.3	19.4	19.4	dB
Input Return Loss		25.2	29.3	27.7	24.8	dB
Output Return Loss		20.7	25.5	29.5	34.2	dB
Output P1dB		18.9	18.5	18.1	17.6	dBm
OIP3	Pout=+0 dBm/tone, Δf=1 MHz	35.4	35.1	35.0	34.9	dBm
Noise figure ⁽¹⁾		0.78	0.79	0.77	0.73	dB

Note:

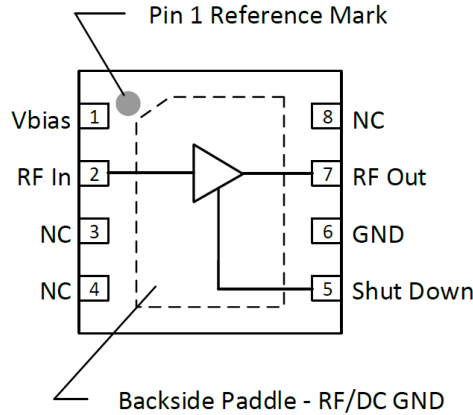
1. With Input trace loss deducted

Performance Plots – QPL9058EVB-01

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 54\text{ mA}$, $50\ \Omega$ system



Pad Configuration and Description

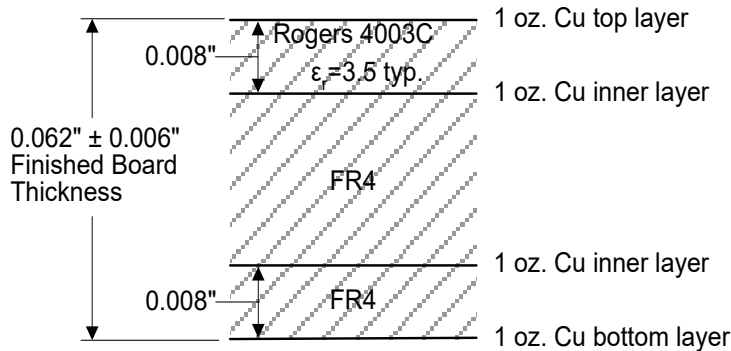


Top View

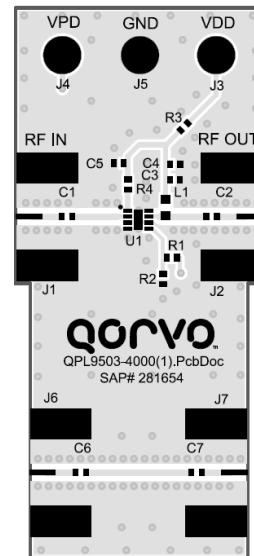
Pad No.	Label	Description
1	V _{bias}	Sets the LNA bias current for the device.
2	RF In	RF Input pin, internally matched to 50 ohms. A DC block is required.
5	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out	RF Output pin, internally matched to 50 ohms. A DC block is required. V _{DD} supply pin.
3, 4, 6, 8	NC	Not connected internally. This pin may be left floating or connected to ground.
Backside Paddle	RF/DC GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are recommended.

Evaluation Board PCB Information

Qorvo PCB Material and Stack-up



50 ohm line dimensions: width = 0.0182", spacing = 0.020"



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020E



Caution!
 ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu (*Thickness: Ni 0.508 ~1.524 μm; Pd 0.023 ~ 0.1016 μm; Au 0.00254 ~ 0.01016 μm*)

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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