PCB Layout Guidelines for QFN Package

1 Abstract

This Application Note provides a set of guidelines for the handling and board mounting of QFN (Quad Flat No-lead) packages, including recommendations for printed-circuit board (PCB) design, soldering, and rework.

2 Introduction

The quad flat no-lead (QFN) is a small size, lead-less plastic package with a low profile, moderate thermal dissipation, and good electrical performance. It is a surface mount package with metallized terminal pads located at the bottom surface of the package. Figure 1. shows the bottom view of a QFN55-40 package.

QFN is also designed with the die attach pad exposed at the bottom side to provide excellent thermal conduction between die and exterior of the package. Heat transfer can be further facilitated by metal vias in the thermal land pattern of the PCB. The exposed pad also enables ground connection. Refer to each IC's DS for its specific exposed pad electrical connection and recommended usage. Figure 2 shows the section view of wire bond QFN package soldered onto a PCB.

QFN is suitable for a broad range of applications in consumer, industrial, and automotive area, including sensor and power applications.

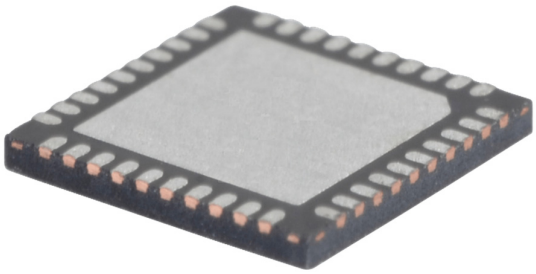


Figure 1. Bottom view of a QFN55-40 package

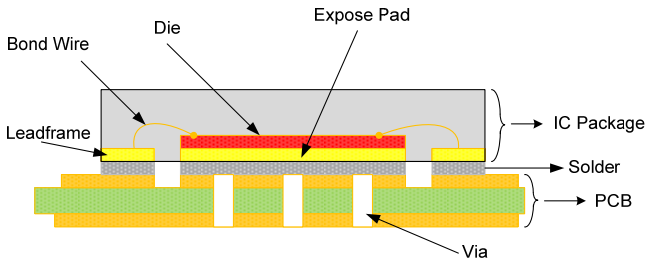


Figure 2. Section view of wire bond package soldered onto a PCB

3 QFN Package Features

3.1 QFN Package Design.

Figures 3 and 4 show the cross-section of typical sawed QFN. Active-Semi has two types of QFN packages: wire bond QFN and FCOL (Flip Chip on Lead) QFN. Both package designs are leadframe based.

Wire Bond QFN: The die is usually glued to the die pad of the leadframe, either with a conductive or nonconductive adhesive. Electrical interconnections from the die to the terminal pads are made with wire bonding. The die pad is exposed external to the package.

Figure 3 shows the cross section view of a typical sawed wire bond QFN package. The final product is sawed from a molded leadframe strip.

Figure 3. Cross section view of a typical wire bond QFN package

FCOL QFN: the flip chip on lead QFN packages enable a near-chip-scale package. The bumped die is flipped and attached to the leadframe. The solder bumps replace the bond wires as the interconnections from die to terminal pads. It allows a larger die to be assembled in the same package size than with using conventional wire bonding.

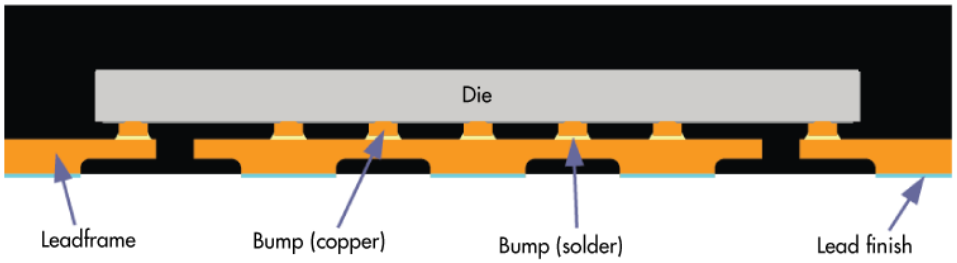


Figure 4. Cross section view of a flip chip QFN package

3.2 Package terminal types

Active-Semi has two different terminal designs for sawed QFN packages: fully-exposed terminal ends QFN and side wettable QFN. These are distinguishable by the geometry of the outer terminal ends. The side wettable QFN provides half of the lead plated on the package side, while standard QFN side is bare copper exposed. Figure 5 shows the cross section view of the difference of the two designs.

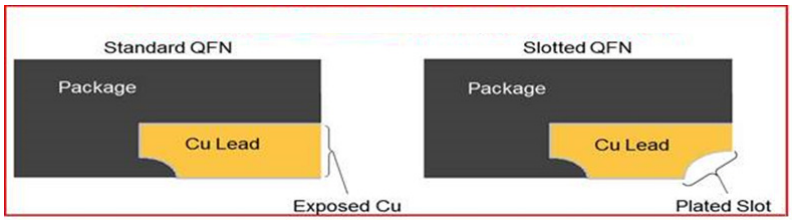


Figure 5. Cross section of standard and side wettable QFN

a) Fully-exposed terminal ends

The fully exposed terminal end is standard package for consumer and industrial products.

There is no plating on the side wall of the leads for Active-Semi standard QFN package because plating process is before package singulation. The side wall of the leads is exposed all the way to the edge of the package when viewed from the bottom of the package. Refer to Figure 6.

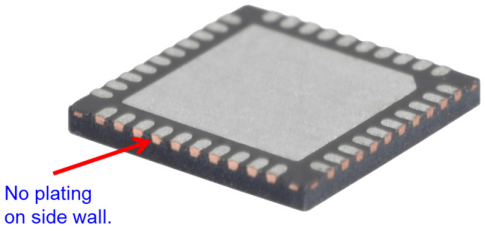


Figure 6. Fully-exposed terminal ends QFN

It is possible that a solder fillet is formed up the side of the component if the terminal end is properly wetted. This may not be the case if the bare copper has been oxidized during Active-Semi dry-bake or during customer storage. Figure 7 shows the actual soldering condition on customer board. The lead is well soldered on the bottom side while the side wall is not wetted.

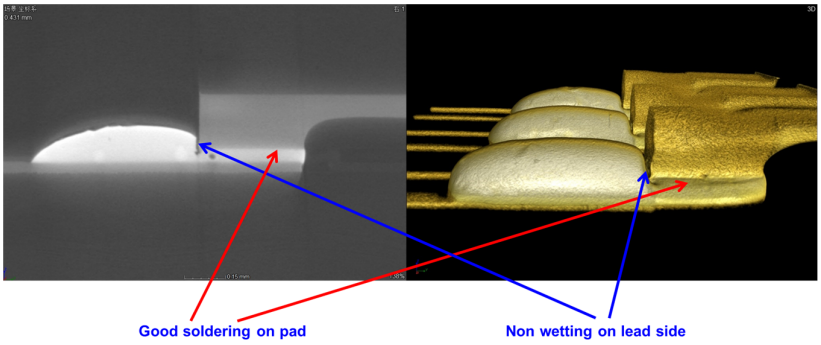


Figure 7. Fully-exposed terminal ends QFN soldering condition

According to IPC-A-610G, there is no requirement for dimension H (Termination Height) for a QFN package without side wall plating. Refer to Figure 8.

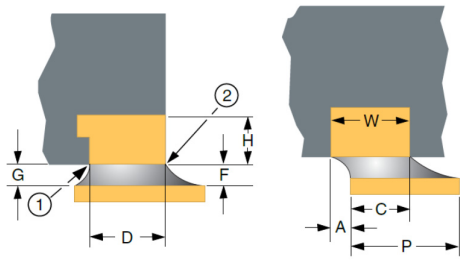


Figure 8. *IPC-A-610G (H) = height of solderable surface of lead, if present. Some package configurations do not have a continuous solderable surface on the sides and do not require a toe (end) fillet.*

b) Terminal ends with Side Wettable Flank (WF)

The Side Wettable Flank is special design for **automotive** products. The Side Wettable Flank QFN is special design for automotive products. A wettable lead end on a QFN promotes wetting of solder to the ends of the QFN terminals during PCB assembly in order to form a solder fillet which is inspectable by AOI (Automated Optical Inspection).

The main features of the wettable lead ends:

- Wettable Flank (WF): the flank (end) of the lead/terminal is created to be wettable.
- INSPECTABLE JOINT (IJ): the lead/terminal ends are created to be wettable to promote a visible, inspectable joint/fillet.
- SOLDERABLE LEAD END: the lead/terminal end is created to allow solder to readily wet to it.
- SIDE SOLDERABLE: the side of the package (I.O.W. lead ends) is created to promote solder wetting.

Figure 9 shows the two typical Active-Semi's WF solutions, step cut and dimple at the terminal ends. The step cut is formed during the package singulation process, while the dimpled terminal is formed during the half-etching step of the leadframe fabrication process. The fillets are formed and should be visible on the PCB after the solder reflow process, as shown in Figure 10 and Figure 11.

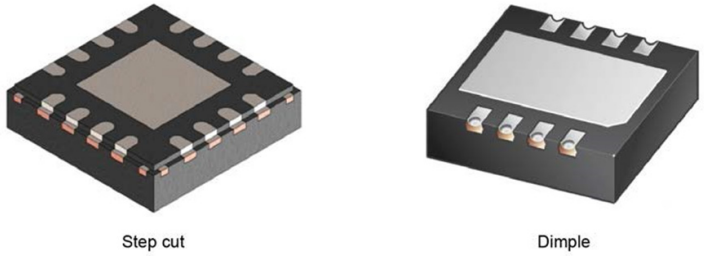


Figure 9. Step cut and Dimple Wettable flank (WF)

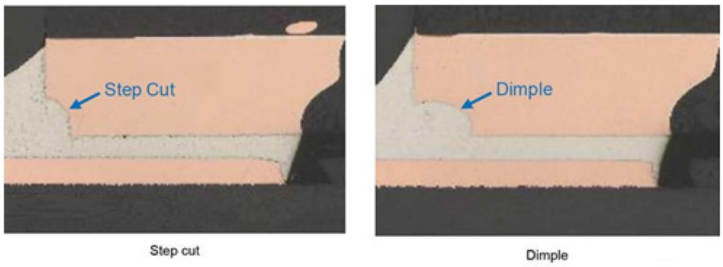


Figure 10. Solder fillets cross-sections after reflow

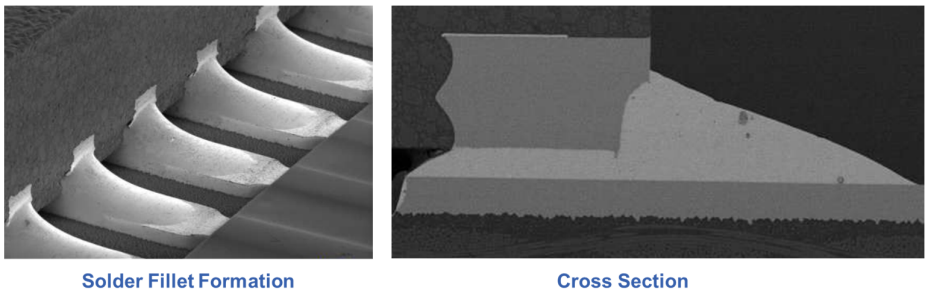


Figure 11. Solder fillet formation with wettable flank

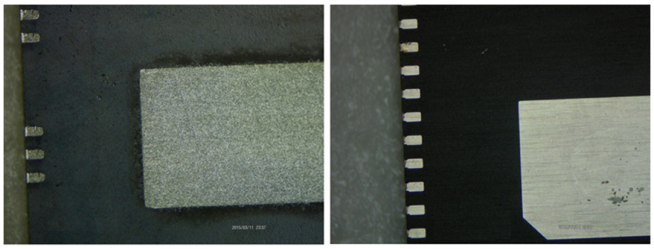
3.3 Leadframe Finishing

Active-Semi provides two types of lead finishing leadframes for QFN packages. There is no difference of the quality and reliability of the products assembled using two types of lead-frames. Both types of leadframes comply with the solderability requirements per J-STD-002. Figure 12 shows the difference of the visual inspection result on two types of lead-frames.

Pre-plated leadframe, the leadframe is plated by leadframe supplier, and sent to assembly house for packaging. The plating material is NiPdAu.

In line plated leadframe, the leadframe is plated in assembly line. The plating material is

pure tin. The step cut solution for side wettable flank uses in line plated leadframe only.



In line plated leadframe. Pre-plated leadframe

Figure 12. Different types of lead finishing

4 PCB design for QFN Package

4.1 Package Dimension

For robust board assembly and board level reliability, the PCB layout and stencil designs are critical to ensure sufficient solder coverage between package and PCB. When designing the PCB layout, please refer to the Active-Semi's package Outline and Dimension drawing in the datasheet to obtain the package dimensions and tolerances. Figure 13 shows an example of a QFN55-40, 0.4mm pitch package outline drawing. The D, E, b, e, L, D2, E2 dimensions are critical to design and layout the PCB.

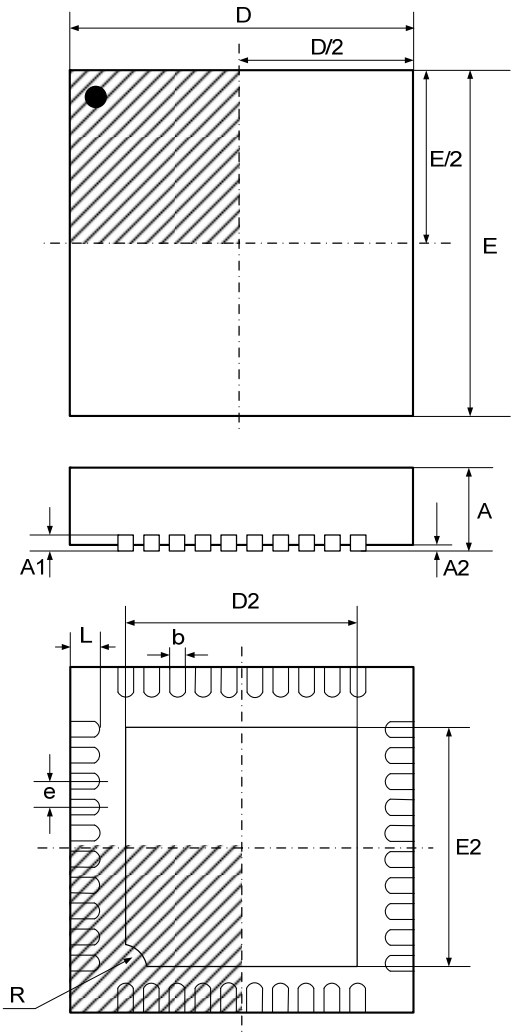


Figure 13. QFN55-40 Package Outline Drawing

4.2 PCB Layout Guidelines

Figure 14 demonstrates how to design the PCB landing pattern for a 5 x 5 mm - 40-pin, 0.4mm -pitch package. The PCB designer needs to design the Pads and Thermal Pad according to the Package Outlines and Dimensions provided in the Active-Semi datasheet. Below are recommended basic calculation for each dimension:

ZDmin = Dmax + 2(0.25)

ZEmin = Emax + 2(0.25)

GDmin = Dmin - 2Lmax - 0.1

GEmin = Emin - 2Lmax - 0.1

PDmax = GDmin - 2CPL where CPL = 0.15

PEmax = GEmin - 2CPL where CPL = 0.15

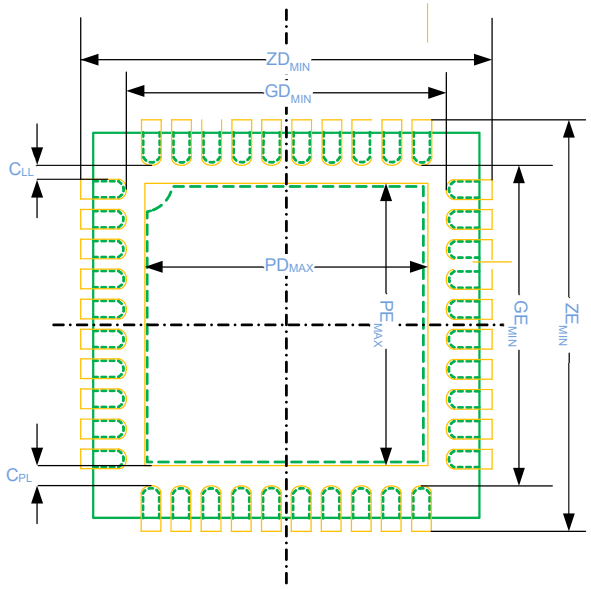


Figure 14. PCB land pattern of a QFN40L Package

4.3 PCB Lead Figure Land Pattern Design

A land is the conductive pattern on the PCB used for the solder connection of a component. In general, the PCB land pattern (footprint) should be designed slightly wider and longer than the IC Exposed Leads.

It follows the generic requirements for surface mount design and land pattern standards from the Institute for Printed Circuits (IPC) document IPC-7351, it includes guidelines for a large number of QFN, based on assumed package dimensions.

The Pad length (Y) should be designed at least 0.3mm longer than the package terminal length (L) for good filleting. The pad length should be extended 0.05mm towards the center line of the package.

The Pad width (X) should be a minimum 0.05mm wider (0.025mm each side) than the package terminal width (b) as shown in Figure 15 below.

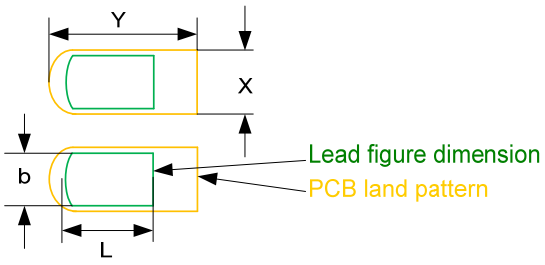


Figure 15. Lead Pads

Notice: PCB designer must keep enough clearance between Lead Pads (CLL) and from Lead Pads to Thermal Pad (CPL) to be minimum 0.15mm to prevent solder bridging.

4.4 PCB Thermal Pad Land Pattern Design

The PCB's Thermal Pad is the exposed copper area which is not covered by the solder mask. This Thermal Pad must be soldered directly to the Exposed Pad on the bottom of the IC. This thermal Pad should be made as large as possible to improve the thermal and electrical characteristics.

Thermal Pad Via Design

Active-Semi highly recommends using multiple vias inside the thermal pad area to conduct heat from the top layer to the inner or bottom layers. Correct layout of these vias greatly improves the thermal characteristics of the IC as well as electrical performance. Figure 16 shows example via placement. The following are dimensional rules for thermal pad area vias:

Pitch: 1mm to 1.2mm pitch

Diameter: 0.3mm to 0.33mm

The number of vias included in a PCB layout is application-specific and depends upon the

package power dissipation and electrical conductivity requirements. Thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias required. Figure 7 shows Active-Semi's recommendations for solid vias which directly connect to copper. Active-Semi does not recommend thermal relief vias.

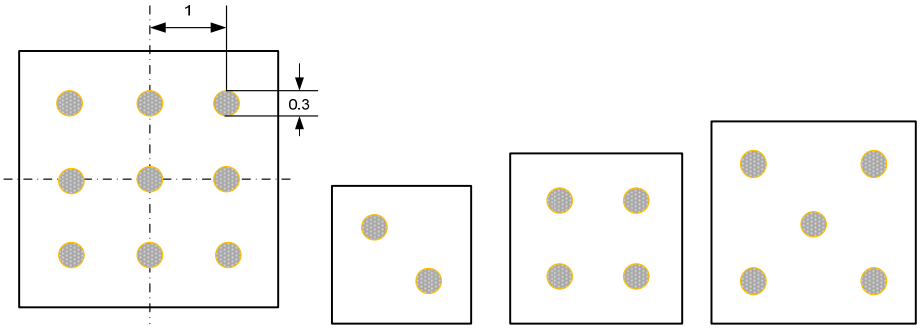


Figure 16. Thermal Via Placement

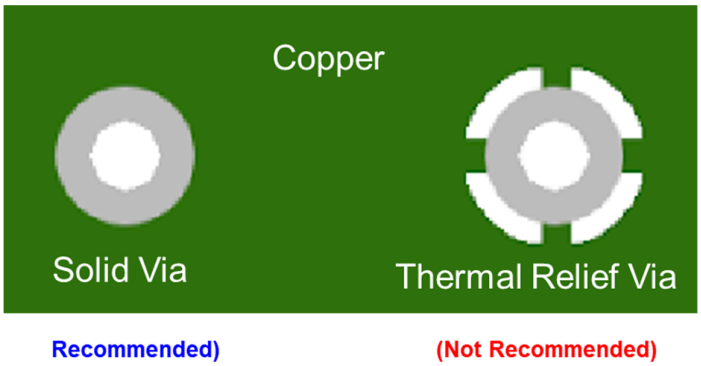


Figure 17. Solid vs Thermal Relief Via

Solder Mask Openings

Pads can be either Non-solder mask defined (NSMD) or solder mask defined (SMD). A NSMD pad is defined by having a metal pad on the PCB that is smaller than the solder mask opening. A SMD pad is defined where the copper is larger than the solder mask opening. In this case, the solder mask opening is smaller than the copper and defines the size of the pad. Active-Semi recommends Non Solder Mask Defined (NSMD) pads when possible.

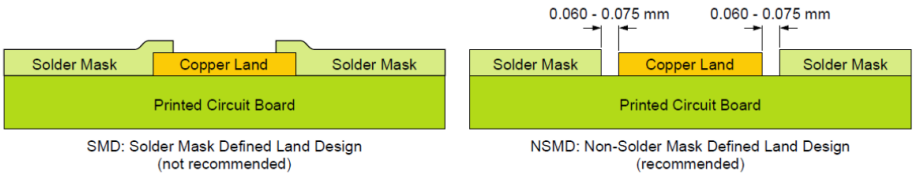


Figure 18. Construction of SMD and NSMD

NSMD pads provide better solder joint reliability. Solder mask should surround each pad, with masking pattern 60 - 70µm larger than the pad size. The solder mask can be designed around each individual lead pad for lead pitches greater than 0.65mm. However, most of the Active-Semi QFN package products use lead-to-lead pitch equal to 0.5mm or smaller. For these packages it is recommended to design the solder mask around all pads on each side. In order to maximize the solder mask between adjacent sides, it is necessary to round the inner corner on each row. This will ensure sufficient solder mask in the corner of the PCB footprint design as shown in the Figure 19 below.

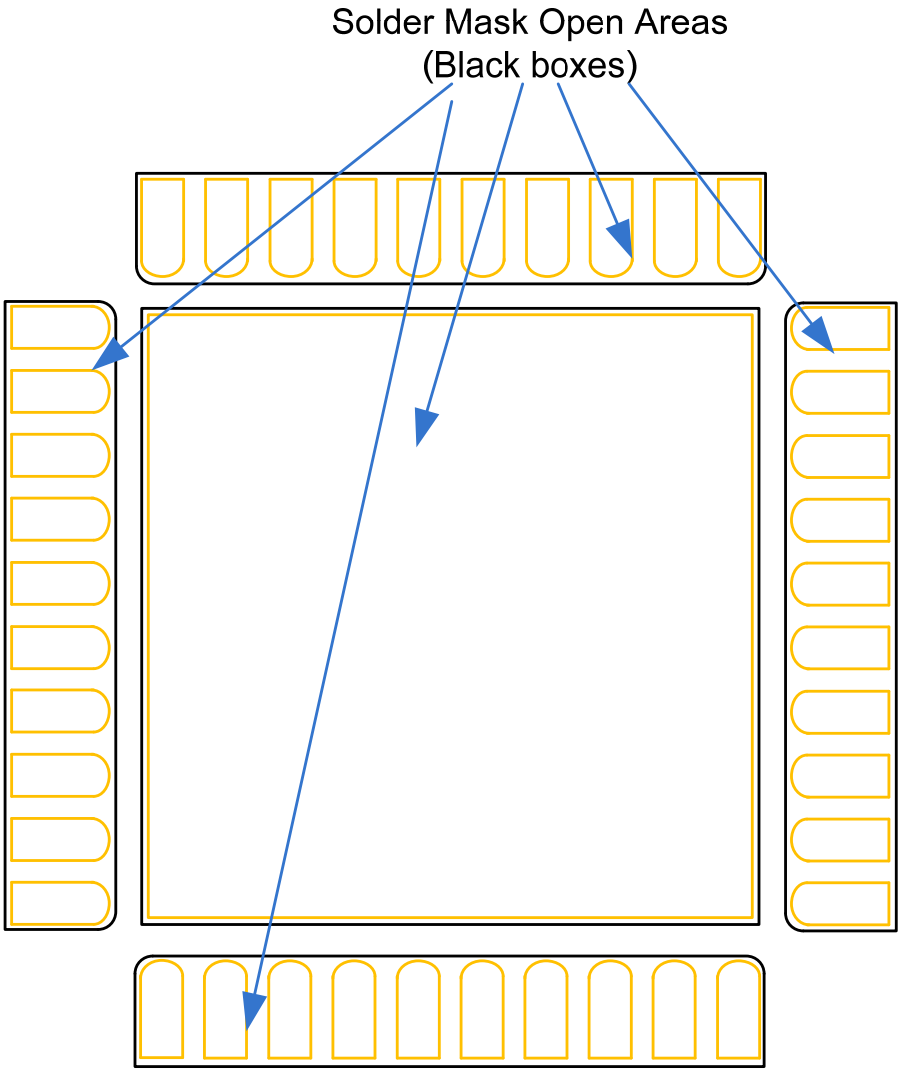


Figure 19. PCB Pads and Solder Mask Opening Design

5 PCB Assembly

5.1 Solder Paste and Stencil

Solder Paste Type

Active-Semi highly recommends customer to use type3 or type 4 solder paste in mounting QFNs to archive high assembly yield. Follow JEDEC/IPC J-STD-20D.1 for standard reflow procedure recommendations.

Paste Type	Sphere Diameter	
	Min. (μm)	Max. (μm)
3	25	45
4	20	38
5	10	25
6	5	15

Flux

Flux is needed to remove surface oxidation, prevents oxidation during reflow and improves the wetting of the solder alloy.

- Rosin-based flux
- Water-soluble flux
- No-clean flux

No-clean flux doesn't require cleaning, but normally a little residue remains on the PCB after soldering.

In general, it is recommended to use a no-clean solder paste, because cleaning of flux residues from underneath the package is not feasible for a QFN-style package (due to the low package standoff).

Solder Stencil for Lead Pads

The stencil aperture opening should be designed to maximum paste release. This is typically accomplished by considering the following two ratios:

- AREA RATIO = Area of Aperture opening / Aperture Wall Area
- ASPECT RATIO = Aperture Width / Stencil Thickness
- Area Ratio should be greater than 0.66.
- Aspect Ratio should be greater than 1.5.

Solder Stencil for Thermal Pads

For large Thermal Pad area with the size larger than 25mm2, Active-Semi recommends using cross-hatching in the thermal pads stencil opening of a QFN package (shown in Figure 20). Cross-hatching will prevent excessive amount of applied solder paste, thus reducing the risk of solder bridging.

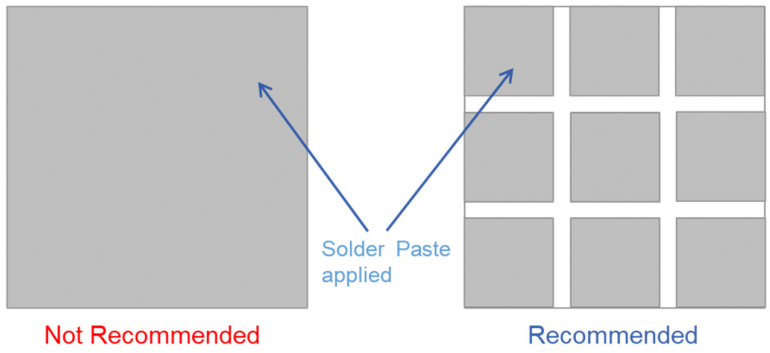


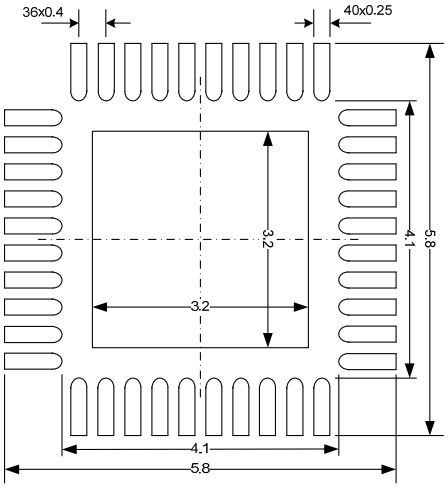
Figure 20. Thermal Pad Stencil Opening for Large Thermal Pad

The primary concern with a full-pad solder-paste application is “floating”—an excessive amount of solder between the thermal pad and the PCB can cause the entire component to float above the level at which the perimeter lands can make contact with their pads.

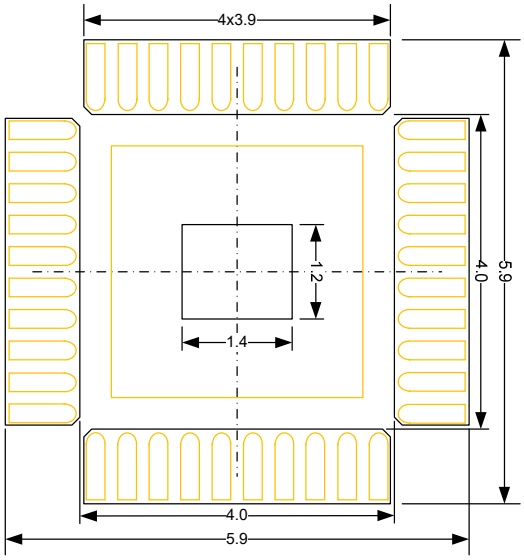
Figure 21. Non-wetting defect with excessive solder on thermal pad

The following pages provide recommended PCB land pattern, thermal vias, solder mask opening, and stencil design for different packages.

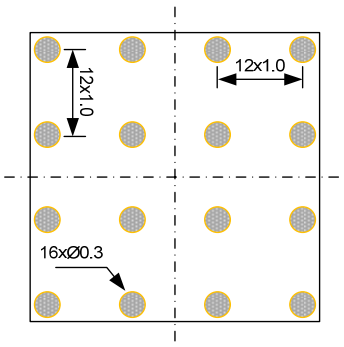
40L-FCSLP EXAMPLE



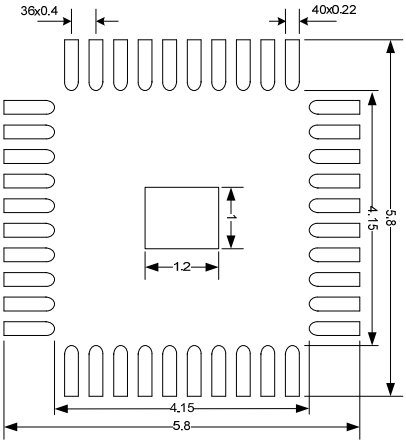
PCB Layout Pattern



Solder Mask Opening



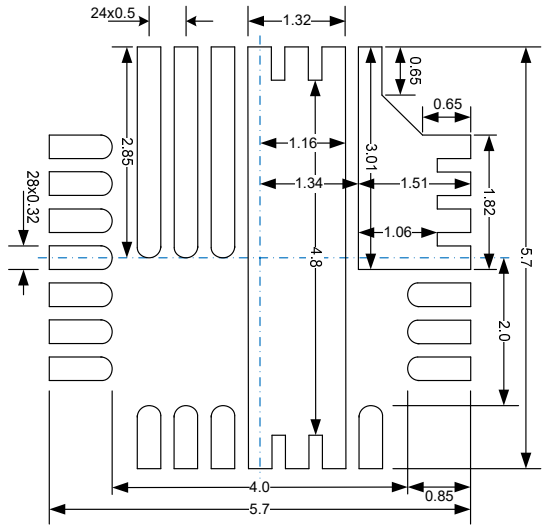
Thermal Vias Design



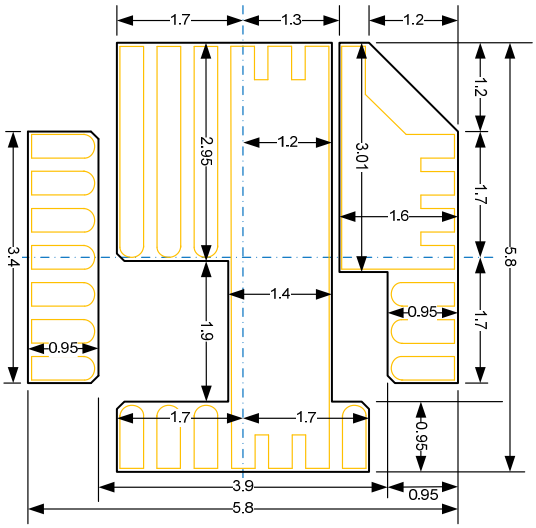
Stencil Design

Note 1: All dimensions are in mm
Note 2: The ACT8870 uses this special package

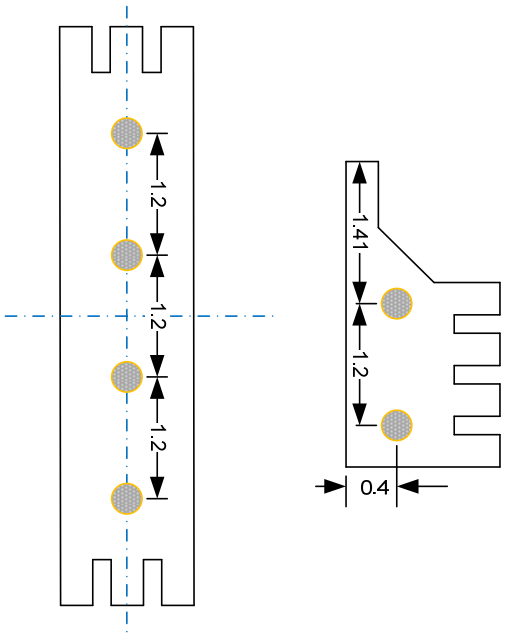
28L-FCSLP EXAMPLE



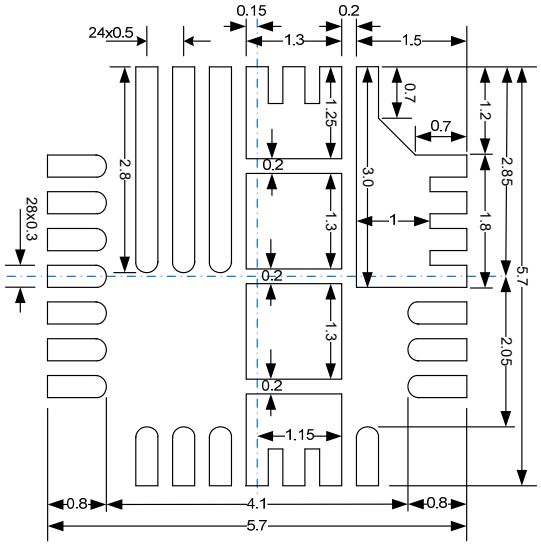
PCB Layout Pattern



Solder Mask Opening



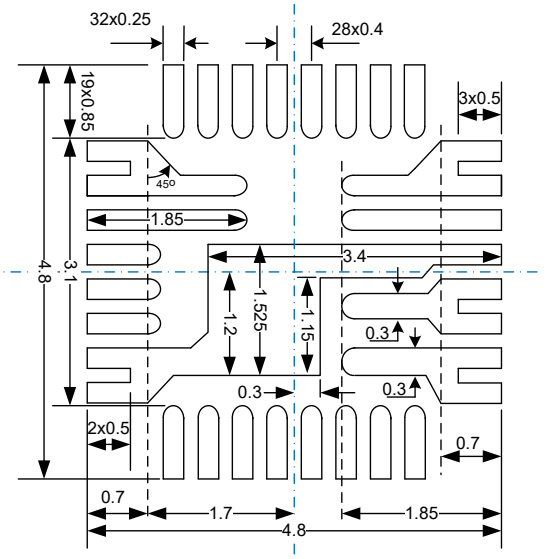
Thermal Vias Design



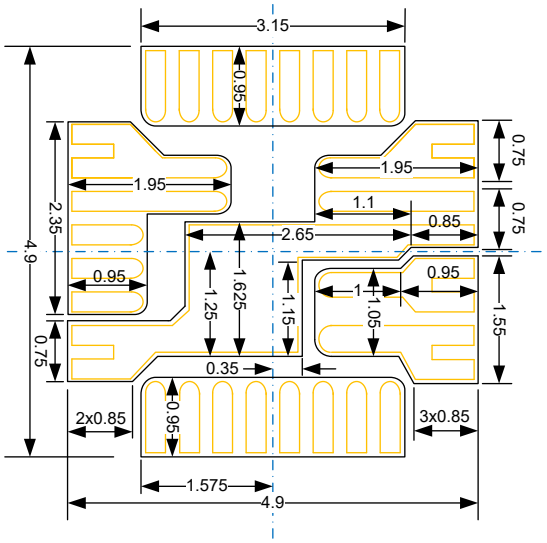
Stencil Design

Note 1: All dimensions are in mm
Note 2: The ACT4910 uses this special package

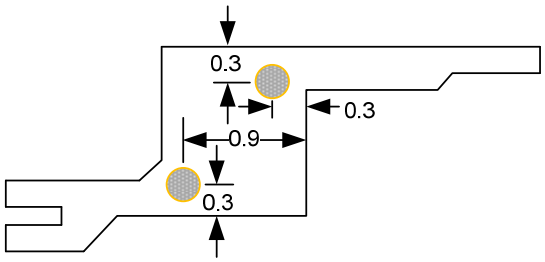
32L-FCSLP EXAMPLE



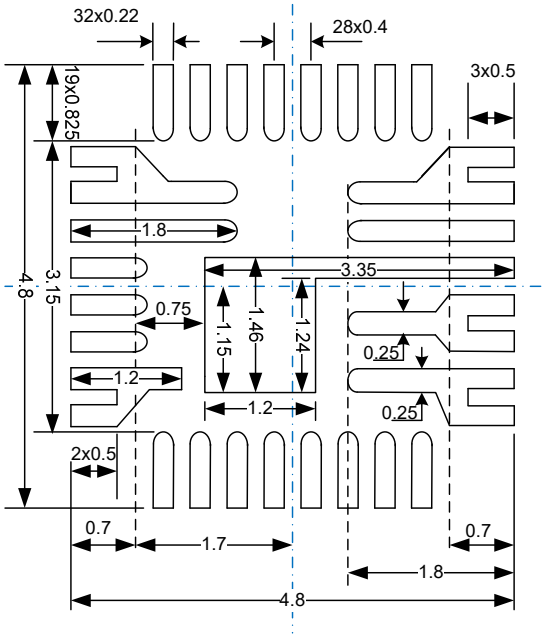
PCB Layout Pattern



Solder Mask Opening



Thermal Vias Design

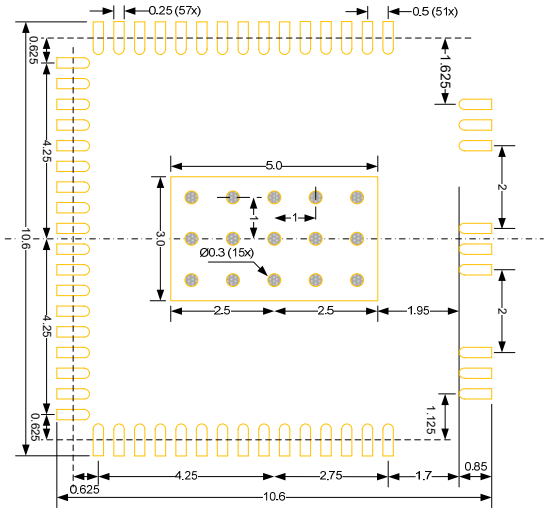


Stencil Design

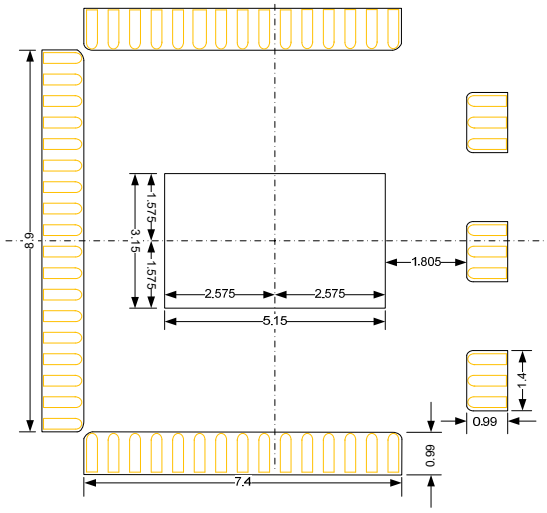
For the Thermal Via Design, the PCB designer may put 4x of 0.3mm vias in the middle pad.

Note 1: All dimensions are in mm
Note 2: The ACT88320 uses this special package

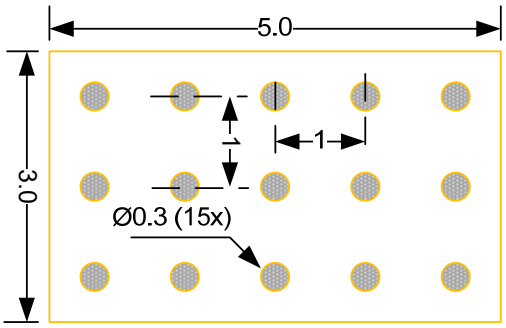
TQFN1010-57 EXAMPLE



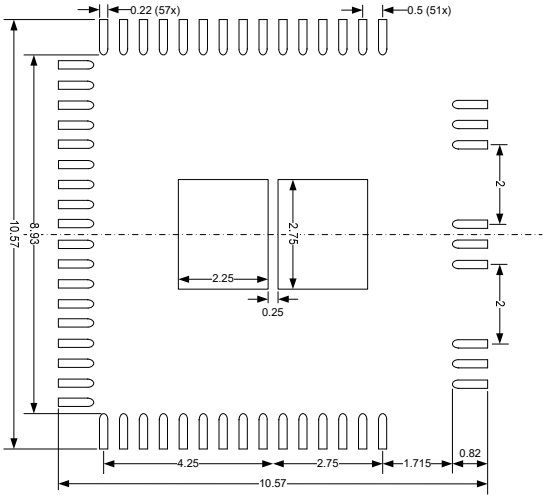
PCB Layout Pattern



Solder Mask Opening



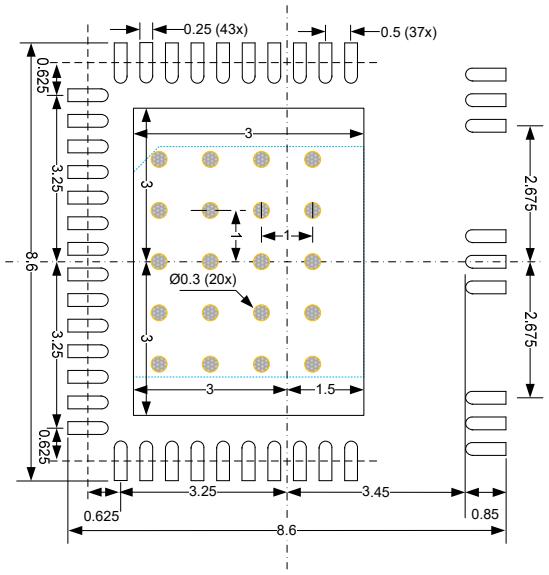
Thermal Vias Design



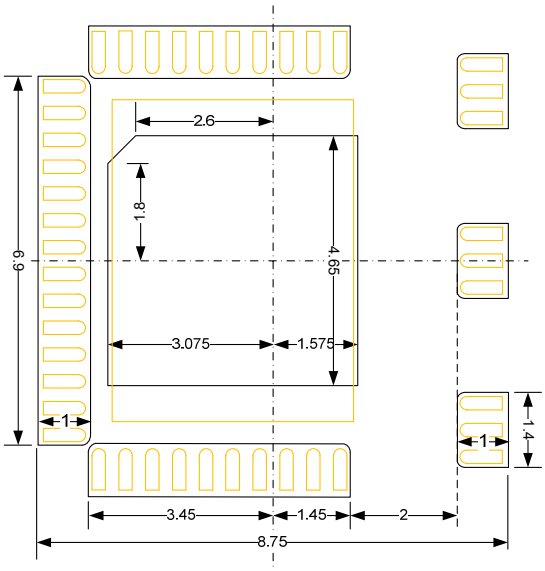
Stencil Design

Note 1: All dimensions are in mm
Note 2: The PAC5250 uses this special package

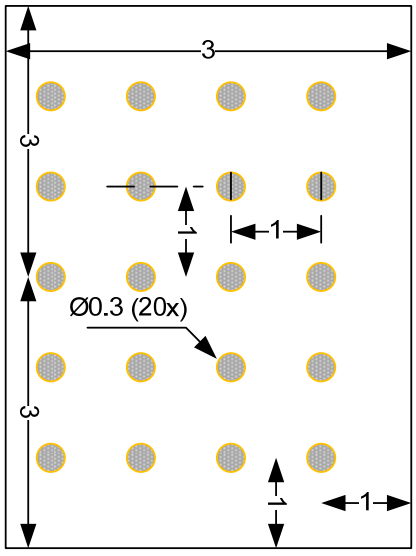
TQFN88-43 EXAMPLE



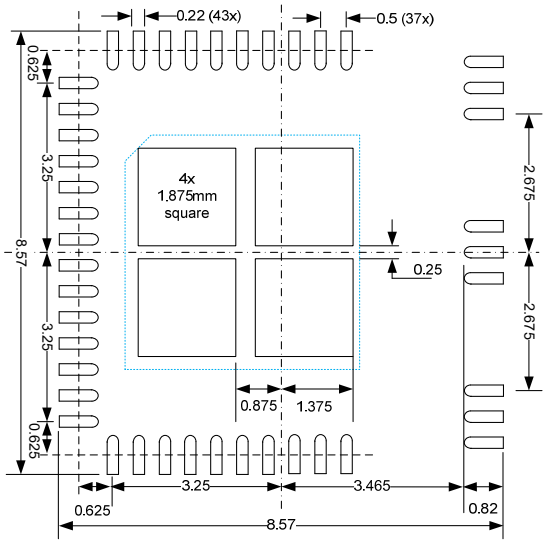
PCB Layout Pattern



Solder Mask Opening



Thermal Vias Design



Stencil Design

Note 1: All dimensions are in mm
Note 2: The PAC5253 uses this special package

Reflow Profile

The temperature profile is the most important control in reflow soldering, and it must be fine-tuned to establish a robust process.

- The actual profile parameters depend upon the solder paste and alloy used; the recommendations from paste manufacturers should be followed.
- Nitrogen reflow is recommended to improve solderability and to reduce defects (like solder balls).

When a board is exposed to the reflow oven temperature, certain areas on the board will heat faster than others depending on the thermal mass and PCB layout. Large components and large copper areas in the board will heat up slower than small components and board areas with little copper.

- The actual temperature on components shall be measured with thermocouples at various places on the PCB surface to ensure that the reflow temperature is reached everywhere on the board.
- It is highly recommended to use the production board to build a thermocouple test board, and then solder the thermal couple sensors on critical component area.

The package top surface temperature shall be monitored at the same time, to validate that the peak package body temperature (TP) does not exceed the MSL classification of individual devices (see IPC/JEDEC J-STD020).

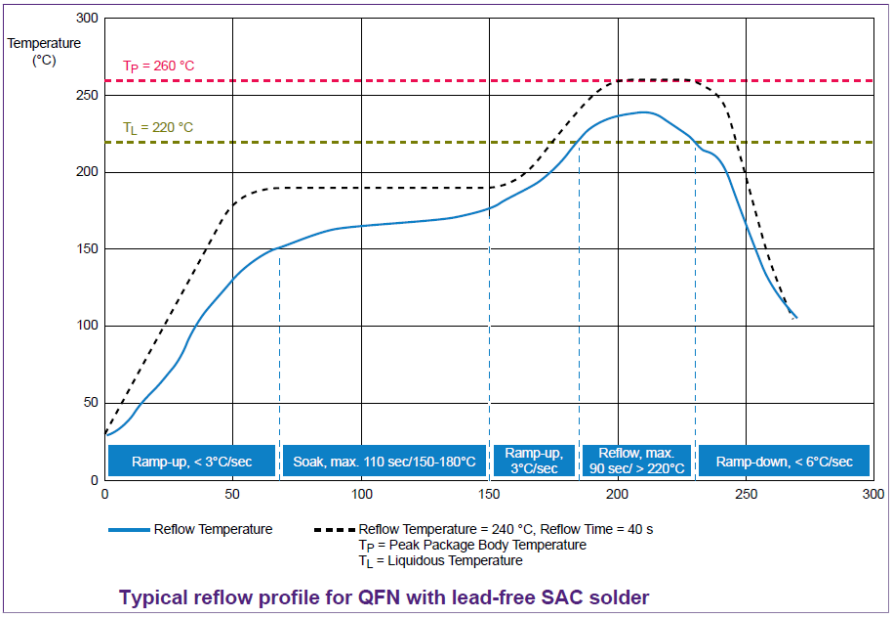


Figure 22. Typical reflow profile for QFN lead free process

Figure 22 shows a typical time/temperature profile (blue) for reflow soldering with lead-free SAC solder alloys using a multi-zone reflow oven. The maximum allowed package body temperature at every stage of the process (depending on the IPC/JEDEC J-STD-020 classification of the package) is represented by the dashed gray line. The reflow profile is divided into five stages:

- **Ramp-up to soak**

  The printed circuit board should be heated evenly to avoid overheating of components. Volatile solvents in the solder paste start to outgas during ramp up. Increasing the temperature too quickly can cause solder balling. The maximum ramp-up rate shall not exceed 3 °C/second to avoid overstress to the package.

- **Pre-heat and soak**

  The PCB assembly is held at 150 to 180 °C for 60 to 120 seconds during thermal soak. The volatiles in the solder paste will be removed and the flux is being activated to reduce oxides from the pads and lands. Time and temperature are recommended by the paste supplier depending on the flux type.

- **Ramp-up to reflow**

  The PCB assembly is uniformly heated above the liquidous temperature of the solder alloy. Again, the maximum ramp-up rate shall not exceed 3 °C/second to avoid overstress to the package.

- **Reflow**

  The recommended peak reflow temperature for SAC alloys shall be > 235 °C. The period above the liquidous temperature (T_L) is called the reflow time. It shall be long enough to allow the liquid solder to uniformly wet the pad and land surfaces and to form an intermetallic phase. Too long of a reflow time may lead to brittle solder joints and could cause damage to the board and components. The peak package body temperature (T_P) must not exceed 260 °C and the time above 255 °C must not exceed 30 seconds, depending on IPC/JEDEC classification.

- **Cool down**

  Fast cool down prevents excess intermetallic formation and creates a fine grain structure of the solder alloy. The ramp-down rate can be faster than the ramp-up, but shall not exceed 6 °C/second to avoid overstress.

  The reflow profile for exposed pad packages need not be any different than the one used for non-thermally/electrically enhanced packages.

  Cross referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact product used.

Special QFN reflow

For some QFN packages with unbalanced pins distribution on 4 sides, the inner stress on the sides are different when the solder paste is melted and solidified again. The unbalanced stress may cause solder cracking on the weak side.

- Make sure the component was placed evenly during SMT.
- When put the board into reflow, place the side with fewer pint in first. Make sure the side with fewer pins is melted and solidified first.
- Optimize the reflow speed.

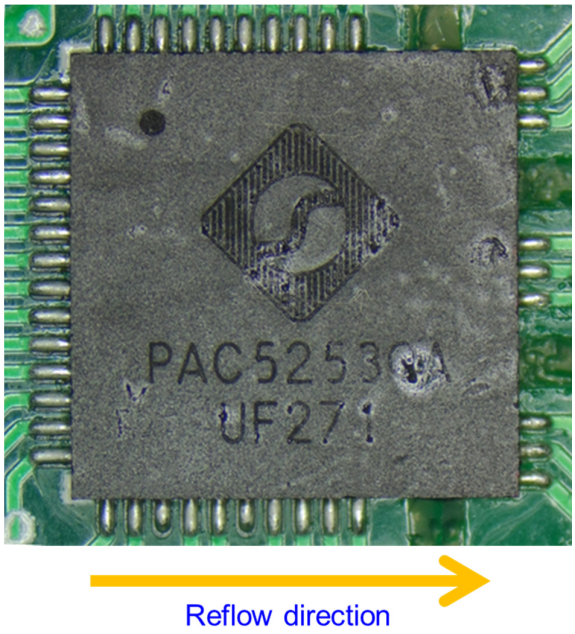


Figure 22. Reflow direction for unbalanced pin layout QFN

6 PCBA Repair and Rework

6.1 Repair

Repairing a single solder joint or the soldered exposed die pad of a QFN package is **not** recommended. The solder joints of the terminals and exposed pad underneath the package cannot be soldered in a controlled way with manual

Active-Semi **doesn't guarantee** the quality and reliability of products that go through a repair process.

6.2 Rework

If a defective component is observed after board assembly, the device can be removed and replaced by a new one. This rework can be performed using the method described in this section.

When performing the rework:

- In any rework, the PCB must be heated. The thermal limits of PCB and components (e.g., MSL information) must be followed.
- During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can damage the component and PCB. To prevent moisture induced failures, it is recommended that the PCB assembly and components have had strict storage control with a controlled environment

such as dry air or nitrogen. In addition, a pre-bake can help to remove the moisture.

- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent packages.
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components.
- Active-Semi follows industry-standard component level qualification requirements, which include three solder reflow passes. The three reflow passes simulate board level attach to a double-sided board and includes one rework pass.
- The removed QFN package should be properly disposed of, so that it is not accidentally mixed with new components.

A typical QFN rework flow process comprises seven stages:

- Tooling preparation
- Component removal
- Site preparation
- Solder paste printing
- Component placement
- Reflow soldering
- Inspection

Note: *Any product that has been removed from PCB board can NOT be reused for the purpose of production. Active-Semi product quality and reliability guaranty/warranty does not apply to the reused products. For any purpose of engineering study, customer should ensure the reused products are scrapped after investigation.*