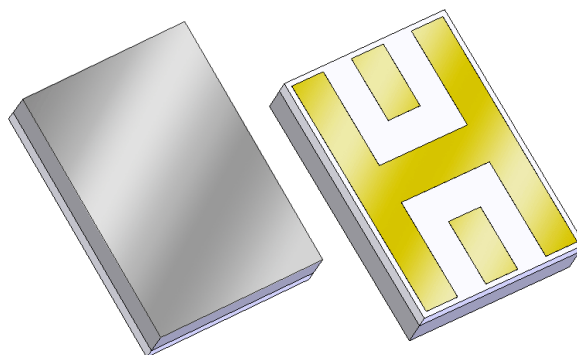


General Description

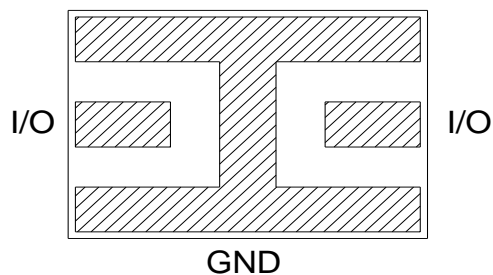
880374 is a 1090 MHz RF Filter designed in a small hermetic package for high selectivity applications.

No matching components are required, making the PCB design and implementation easy.



CSP: 3.74 X 2.59 X 0.889 mm

Functional Block Diagram



Bottom View

Product Features

- Usable bandwidth 16 MHz
- Low Insertion Loss
- High Selectivity
- Single-Ended Operation
- No External Matching Requested
- 50 Ω Impedance at Input / Output
- Ceramic Chip-Scale Package (CSP)
- Small Size
- Hermetically Sealed
- **RoHS** Compliant, **Pb**-Free

Performance is typical across frequency. Please reference electrical specification table and data plots for more details

Applications

- For SSR/IFF Applications
- For High Selectivity Applications

Pin Configuration - Single Ended

Pin No.	Label
I/O	Input / Output
GND	Ground

Ordering Information

Part No.	Description
1062367	880374 1090 MHz IFF BAW Filter
1072909	880374 Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 100°C
Operation Temperature	-40 to 85°C
RF Input Power ⁽¹⁾ - Test conditions: PW = 200ms; DC = 50% @ +25 °C	42 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

⁽¹⁾ Input Power for both Input & Output ports

Minimum Lifetime Ratings

Conditions	Rating
RF Input Power ⁽¹⁾ , Pin 1 & Pin 2	>10K hours

⁽¹⁾ Input Power: CW, 24 dBm, @ +71 °C

Electrical Specifications ^(1,2)

Test conditions unless otherwise noted: Temperature Range = -40 °C to +85 °C, 50 Ω system

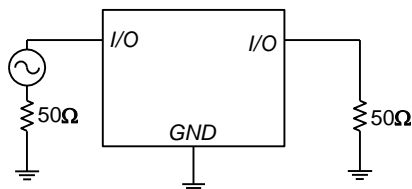
Parameter ⁽³⁾	Conditions	Min	Typical ⁽⁴⁾	Max	Units
Center Frequency (Fo)		-	1090	-	MHz
Maximum Insertion Loss	@ Fo	-	3.0	4.0	dB
3 dB Lower Frequency Edge	Reference to Loss @ Fo	-	-	1082	MHz
3 dB Upper Frequency Edge	Reference to Loss @ Fo	1098	-	-	MHz
40 dB Lower Frequency Edge	Reference to Loss @ Fo	1067.5	1073.0	-	MHz
40 dB Upper Frequency Edge	Reference to Loss @ Fo	-	1107.0	1112.5	MHz
VSWR	@ Fo	-	1.7:1	2.0:1	
Source Impedance ⁽⁵⁾	Single Ended	-	50	-	Ω
Load Impedance ⁽⁵⁾	Single Ended	-	50	-	Ω

Notes:

1. All specifications are based on the Qorvo schematics for the reference designs shown on page 3.
2. In production, devices will be tested at room temperature to a guard banded specification to ensure electrical compliance over temperature.
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacture tolerances.
4. Typical values are based on average measurements at room temperature on pcb. (25 °C ±5 °C)
5. Optimum impedance to achieve the performance shown.

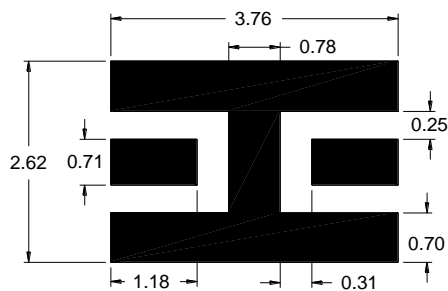
Matching Schematics

50 Ω
 Single-ended
 Input



50 Ω
 Single-ended
 Output

Recommended PCB Mounting Pattern

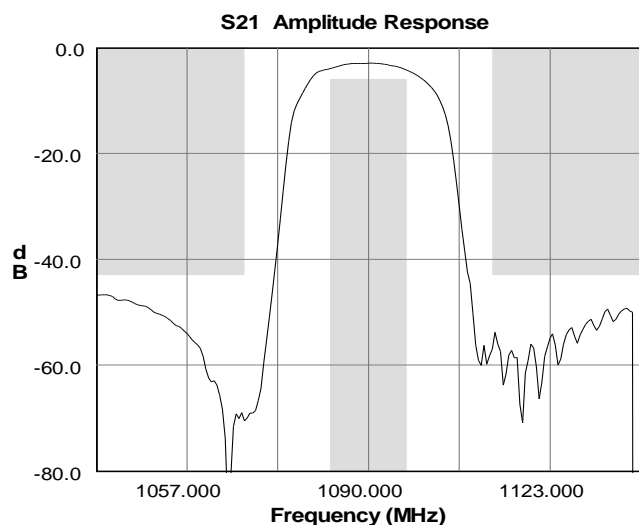


Notes:

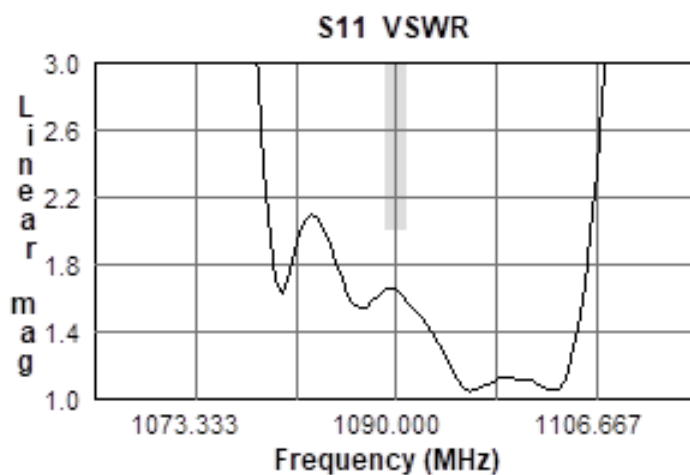
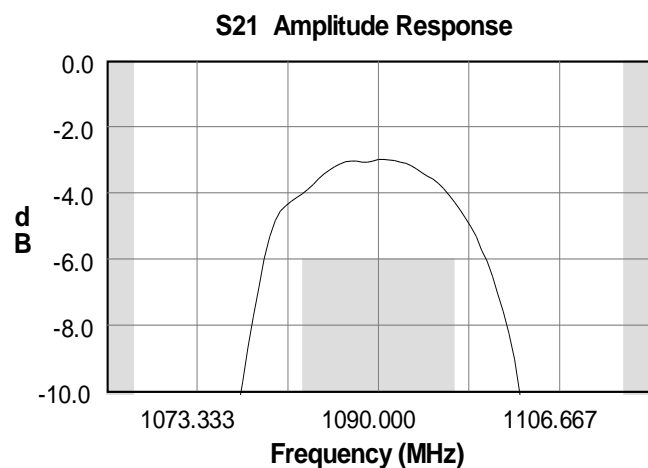
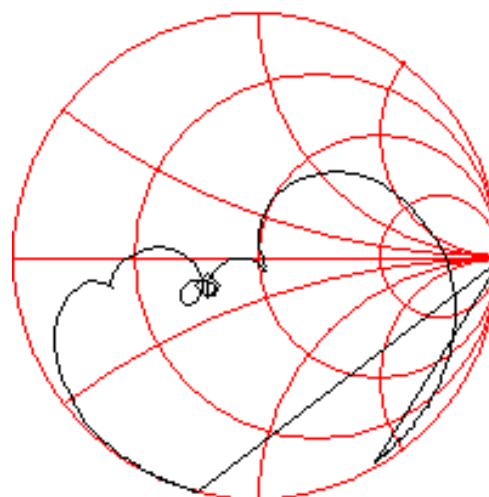
1. All dimensions are in millimeters.
2. Modifications may be necessary to suit end user assembly materials and processes.

Typical Performances

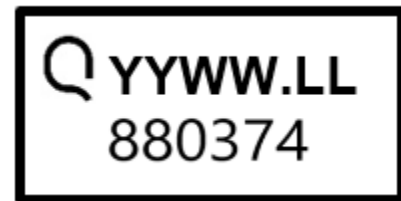
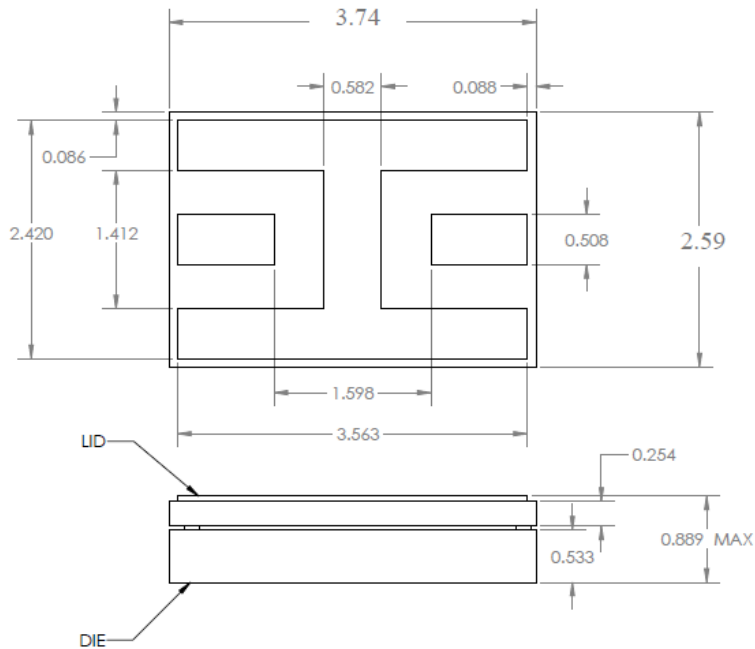
Test conditions unless otherwise noted: Temp = +25 °C ±5 °C, 50 Ω system



S11 Smith Chart



Device Package Information, Marking and Dimensions



Package Style: CSP
Dimensions: 3.74 x 2.59 x 0.889 mm

Package Base: Sapphire
Package Lid: Alumina
Terminations: Au plating over Ni (2.0 - 6.0 μm Ni, 0.33 – 0.83 μm Au)

All dimensions shown are nominal in millimeters.
All tolerances are $\pm 0.13\text{mm}$ except overall length and width $\pm 0.25\text{mm}$.
Overall width, length, and thickness are the only critical dimensions. All other dimensions are for reference only.

Marking includes corporate logo, date code, and product part number.
The date code consists of, YY = last 2 digits of the year, WW = 2 digits of calendar work week and LL = Lot ID, unique lot identifier.
Marking Diagram is for Reference Only.

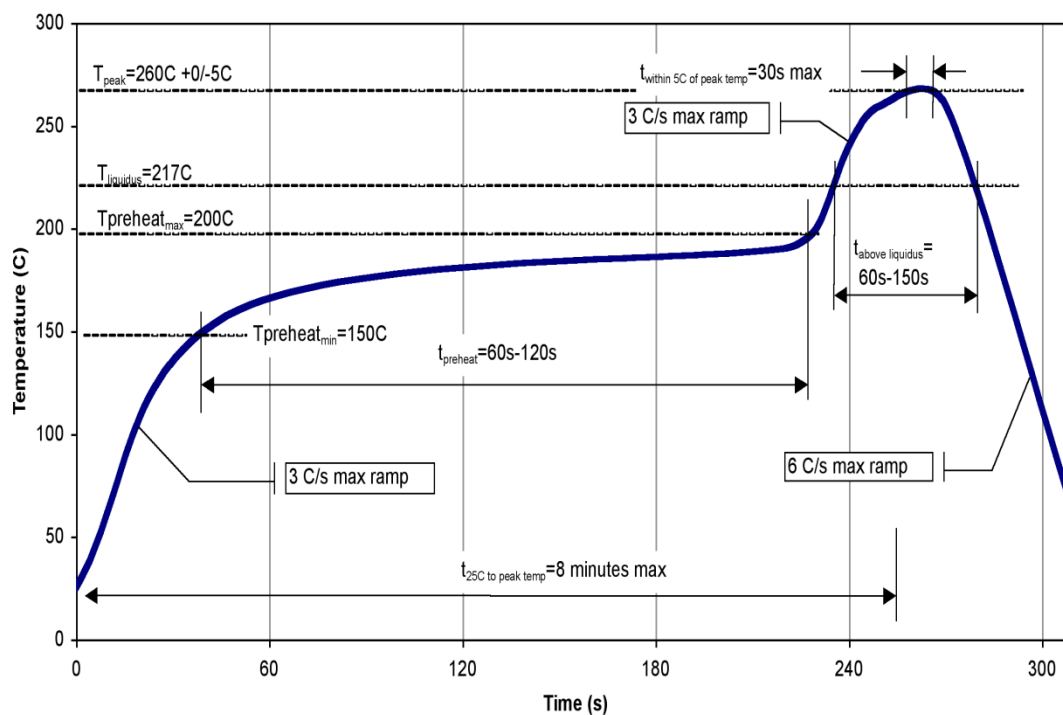
Packaging Information

- Tape and Reel per EIA-481 available. 7" Reel. Additional information available upon request.
- Solder tinning available per IPC J-STD-001.

Assembly Notes

1. Compatible with both Lead-free solder (260°C peak reflow temperature) and tin/lead (245°C peak reflow temp.) soldering processes.
2. Contact plating: Au plating over Ni.

Recommended Soldering Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 3B	ESDA / JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	ESDA / JEDEC JS-002
MSL – Moisture Sensitivity Level	N/A, Hermetic Package	



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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