

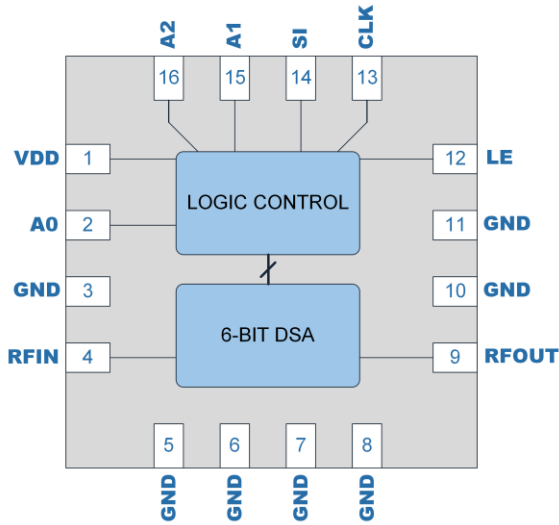
### 1. Product Overview and Benefits

The Qorvo® RFSA3613 is a 6-bit digital step attenuator (DSA) that features high linearity over the entire 31.5dB gain control range with 0.5dB steps. The RFSA3613 uses serial control interface. The RFSA3613 has a low insertion loss of 1.4dB at 2GHz. The patented circuit architecture provides overshoot-free transient switching performance. External address pins allow up to eight DSAs to be controlled on a single bus. RFSA3613 is in a 3mm x 3mm QFN package.



16 Pin 3 x 3 x 0.85mm QFN Package

### 2. Functional Block Diagram



Top View

### 3. Key Features

- 6-bit, 31.5dB Range, 0.5dB Step
- Patented Circuit Architecture
- Overshoot-free Transient
- Frequency Range 50MHz to 6000MHz
- High Linearity, IIP3 <55dBm
- Serial Control Interface
- Fast-Short Switching Time, <120nsec Typical
- Serial Addressable Supports Up to Eight Addresses
- Single Supply 3V to 5V Operation
- RFIN and RFOUT with DC Potential 0 Volt
- Power-up Default Setting is at Maximum Attenuation

### 4. Applications

- Base Stations
- Point-to-Point
- WiFi
- Test Equipment

### 5. Ordering Information

Part Number	Description
RFSA3613TR7	7" T&R with 2500 pieces
RFSA3613PCK-410	50MHz-6GHz PCBA with 5-piece sample bag

## 6. Electrical Characteristics

### 6.1. Absolute Maximum Ratings

Parameter	Conditions	Rating
Storage Temperature		-40°C to 150°C
VDD		-0.5 to +6.0V
All Other DC and Logic Pins	VDD supply voltage Must be applied first	-0.5 to +6.0V
RF input power at RFIN, Max	CW, Tcase +85°C	+30dBm
RF input power at RFOUT, Max		+27dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

### 6.2. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
VDD	+2.7	+5.0	+5.5	V
RF Input Power at RFIN, CW, +85°C			27	dBm
RF Input Power at RFOUT, CW, +85°C			20	dBm
T <sub>CASE</sub>	-40	+25	+105	°C
T <sub>j</sub> for >10 <sup>5</sup> hours MTTF			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

### 6.3. Electrical Specifications

Parameter	Conditions <sup>(1)</sup>	Min.	Typ.	Max.	Units
Operational Frequency Range		50		6000	MHz
Test Frequency			2000		MHz
Insertion Loss <sup>(2)</sup>	0dB attenuation setting		1.4		dB
Attenuation Range	0.5dB step size		31.5		dB
Absolute Attenuation Error			±(0.2+4%)		dB
Return Loss			15		dB
Input IP3			55		dBm
Input P0.1dB			30		dBm
Switching Time	50% control to 10% or 90% RF output		120		ns
Successive Step Phase	At 2000MHz		2		Deg
VDD Current	VDD +5.0V		180		µA
Digital Logic Input High		1.17			V
Digital Logic Input Low				0.63	V
Control Logic Input Current			100		µA
Switching Time	Control Threshold to 90/10% RF, 2GHz			500	ns
Settling Time	Control Threshold to 0.1dB Steady State Error			1000	ns
Thermal Resistance	At maximum attenuation state with RF power applied to the RFIN		55		°C/W

Notes:

1. Test conditions unless otherwise noted: VDD +5.0V, Temp +25°C, 50Ω RF system impedance
2. PCB trace loss deducted

## 7. [Truth | Logic] Table

### 7.1. Attenuation Control Logic Truth Table

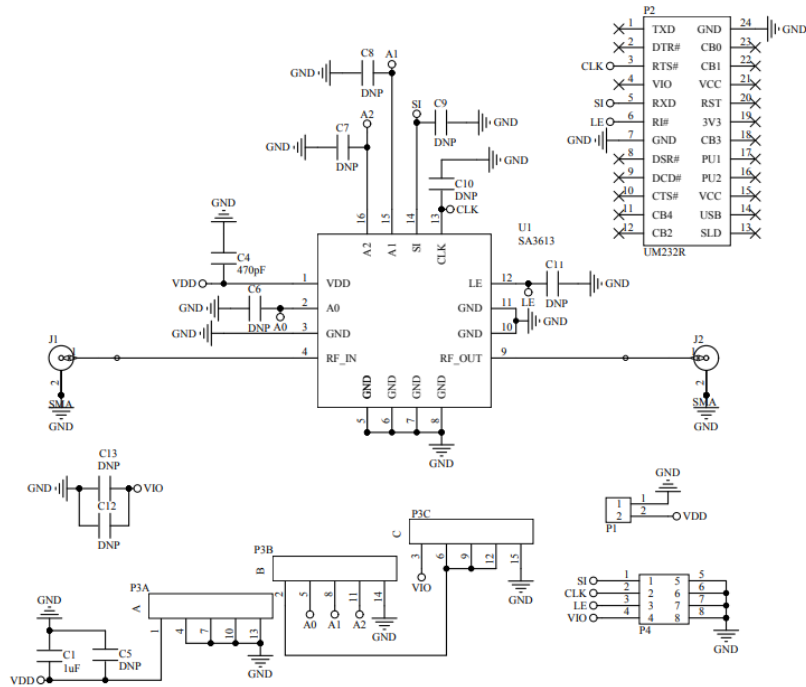
Attenuation Word								Attenuation State
D7	D6	D5	D4	D3	D2	D1 (LSB)	D0	
X	L	L	L	L	L	L	X	0dB / Reference Insertion Loss
X	L	L	L	L	L	H	X	0.5dB
X	L	L	L	L	H	L	X	1.0dB
X	L	L	L	H	L	L	X	2.0dB
X	L	L	H	L	L	L	X	4.0dB
X	L	H	L	L	L	L	X	8.0dB
X	H	L	L	L	L	L	X	16.0dB
X	H	H	H	H	H	H	X	31.5dB

### 7.2. Device Address Truth Table

Address Word								Address
A7	A6	A5	A4	A3	A2 (MSB)	A1	A0	
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

## 8. Application Information

### 8.1. Evaluation Board Circuit Schematic



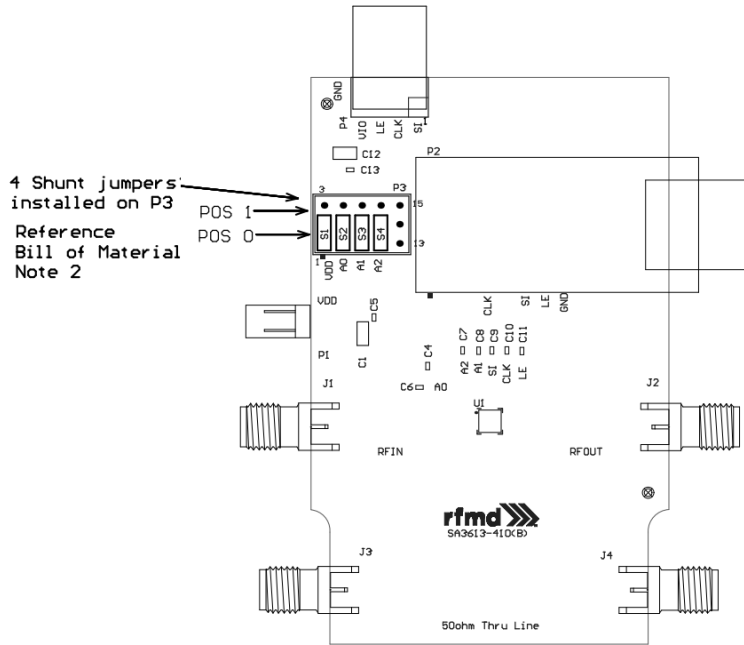
### 8.2. Evaluation Board Bill of Material

Ref. Des.	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board	-	-
U1	-	DSA, 50-6000MHz Digital Step Attenuator	Qorvo	RFSA3613
C1	100pF	CAP, 1µF, 10%, 25V, X7R, 1206	Taiyo Yuden	CE TMK316BJ105KL-T
C4	470pF	CAP, 470pF, 5%, 50V, COG, 0402	Murata	GRM1555C1H471JA01D
J1, J2	SMA	CON, SMA, EL FLT VIPER MAT-21-1038	Amphenol	901-10425
M1	-	MOD, USB TO SERIAL UART, SSOP-28	Future Tech	UM232R
P1	-	CON, HDR, ST, PLRZD, 2-PIN, 0.100"	ITW Pancon	MPSS100-2-C
P2	-	CON, SKT, 24-PIN DIP, .600", T/H	Assmann	AR-24-HZL/01-TT
P3	-	CON, HDR, ST, 3x5, 0.100", T/H	SAMTEC INC.	TSW-105-07-L-T
P4	-	CON, HDR, 2 X 4, RA, .100, T/H	SAMTEC INC.	TSW-104-08-G-D-RA
S1, S2, S3, S4	-	JMP, 2-PIN, 0.100"	3M	929950-00

**Notes:**

1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2
2. Jumpers S1-S4 installed on P3

### 8.3. Evaluation PCBA



EVB Assembly Top View

### 8.4. Application EVB Jumper Configurations

Jumper	Connector	Signal	Position	Connection	Comment
S1	P3	VDD	<b>0</b>	<b>P1 VDD</b>	Device Address Configurations
			1	P4 VIO	
S2		A0	<b>0</b>	<b>GND</b>	
			1	VDD	
S3		A1	<b>0</b>	<b>GND</b>	
			1	VDD	
S4		A2	<b>0</b>	<b>GND</b>	
			1	VDD	

Notes:

1. Default jumper settings are in **BOLD**

## **8.5. Evaluation Board Programming**

### **8.5.1. Using USB Interface**

All jumper configurations on the evaluation board are set to the default values indicated in the table. Refer to the Control Bit Generator (CBG) Software Reference Manual for detailed instructions on how to setup the GUI (Graphic User Interface). Apply the supply voltage to P1. Select 'RFSA3613' from the Parts List of the CBG user interface. Set the attenuation value using the CBG user interface. The attenuator is set to the desired state and measurements can be taken. Note that the external address bits must all be set to '0' when using the USB interface as the CBG software does not have the capability to set the external address in the serial data stream at this time.

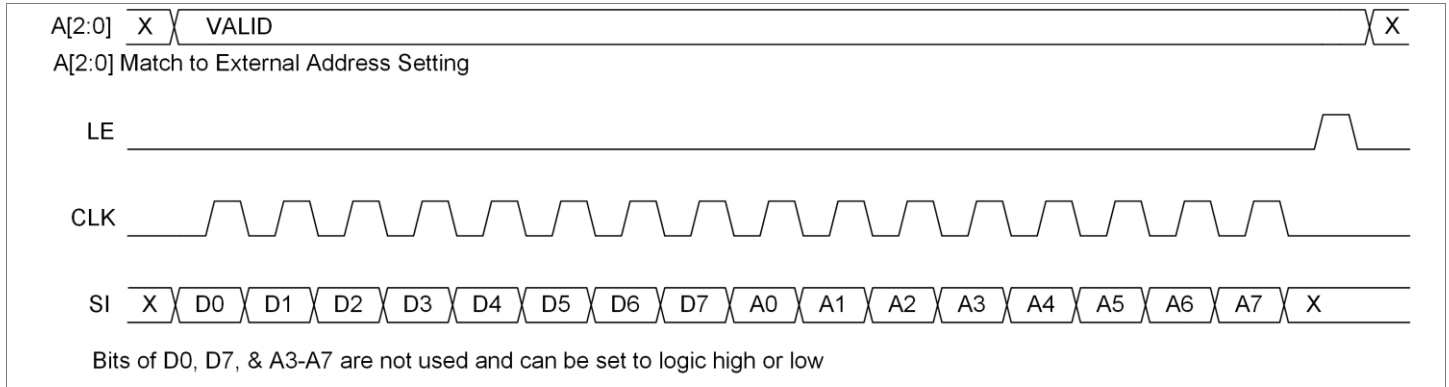
### **8.5.2. Using External Bus**

This configuration allows the user to control the attenuator through the P4 connector using an external harness. Remove the USB interface board if it is currently installed on the evaluation board. Connect a user-supplied harness to the P4 connector. Note that the top row of P4 contains the serial bus signals and the bottom row is ground. Programming jumper S1 is set to '0'. External address jumpers S2 through S4 can be set to any value desired by the user. Apply the supply voltage to P1. Send the appropriate signals onto the serial bus lines in accordance with the Serial Addressable Mode Timing Diagram. The attenuator is set to the desired state and measurements can be taken.

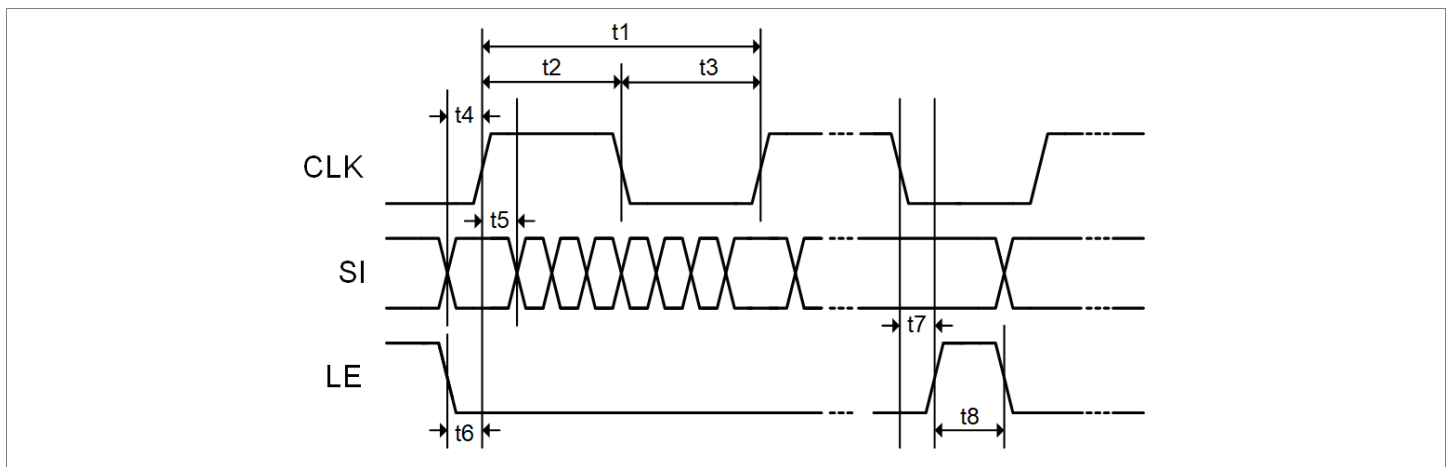
### **8.5.3. Default Power-up Attenuation State**

This default attenuation state is maximum (31.5dB) when supply voltage is applied to the attenuator. The LE signal must be held to logic '0' during power-up.

## 9. Series Bus Timing Diagram

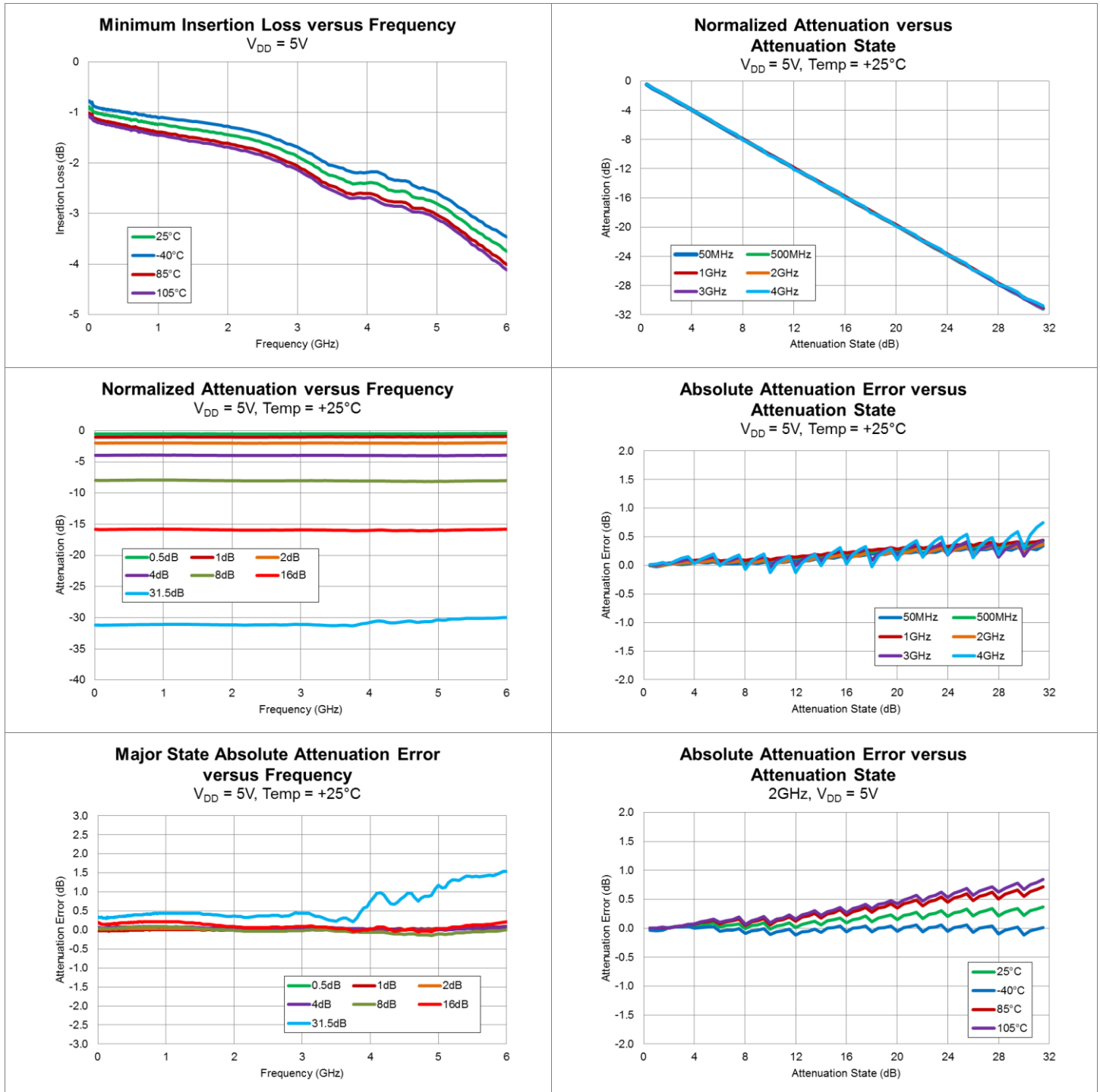


## 10. Series Bus Timing Specifications

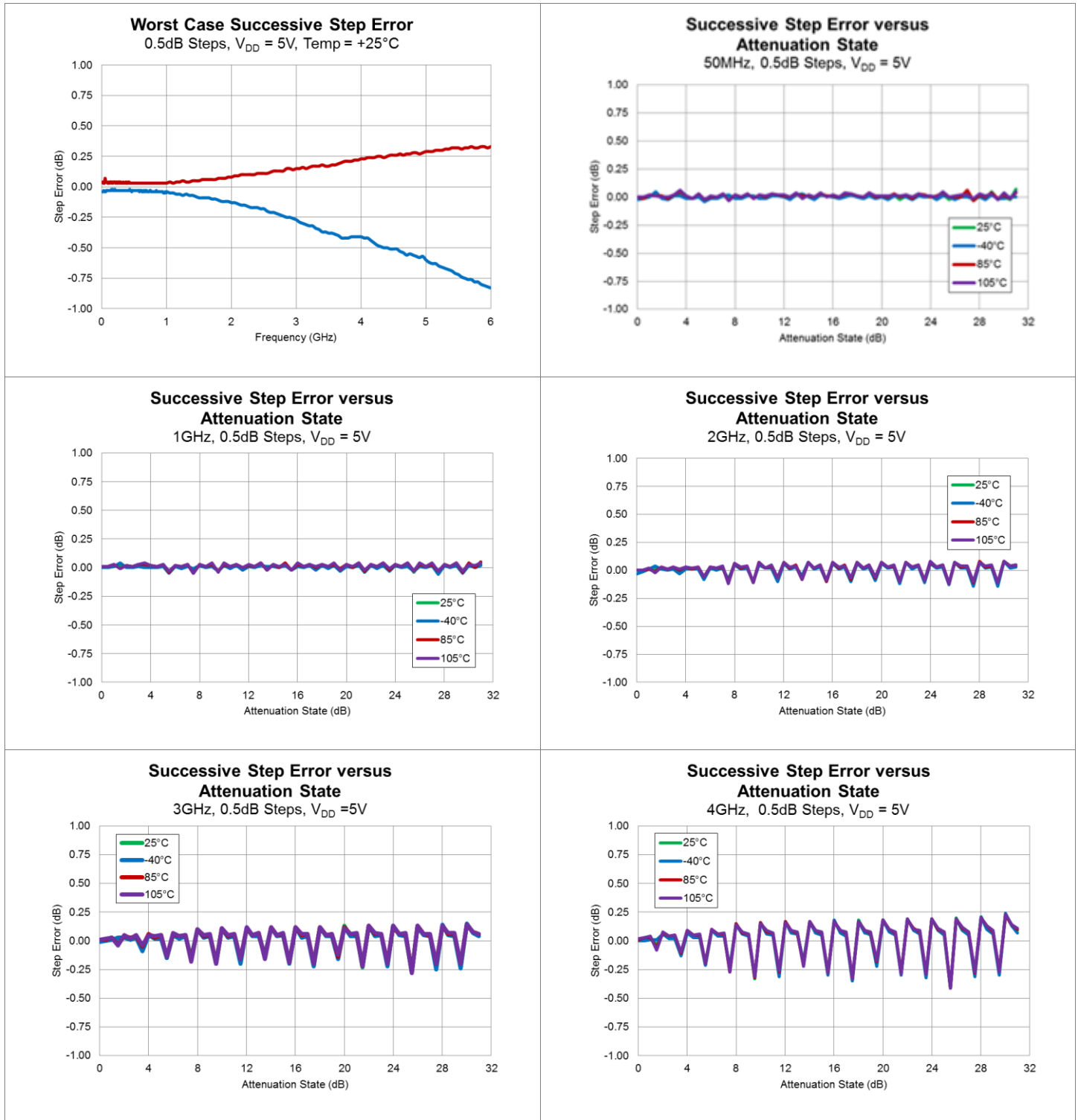


Parameter	Symbol	Min.	Max.	Unit
CLK Frequency	1/t1		25	MHz
CLK High Time	t2	20		ns
CLK Low Time	t3	20		ns
SI Setup Time	t4	5		ns
SI Hold Time	t5	5		ns
LE Low Setup Time	t6	5		ns
LE High Setup Time	t7	5		ns
LE High Time	t8	10		ns

## 11. Typical Performance Plots (1)

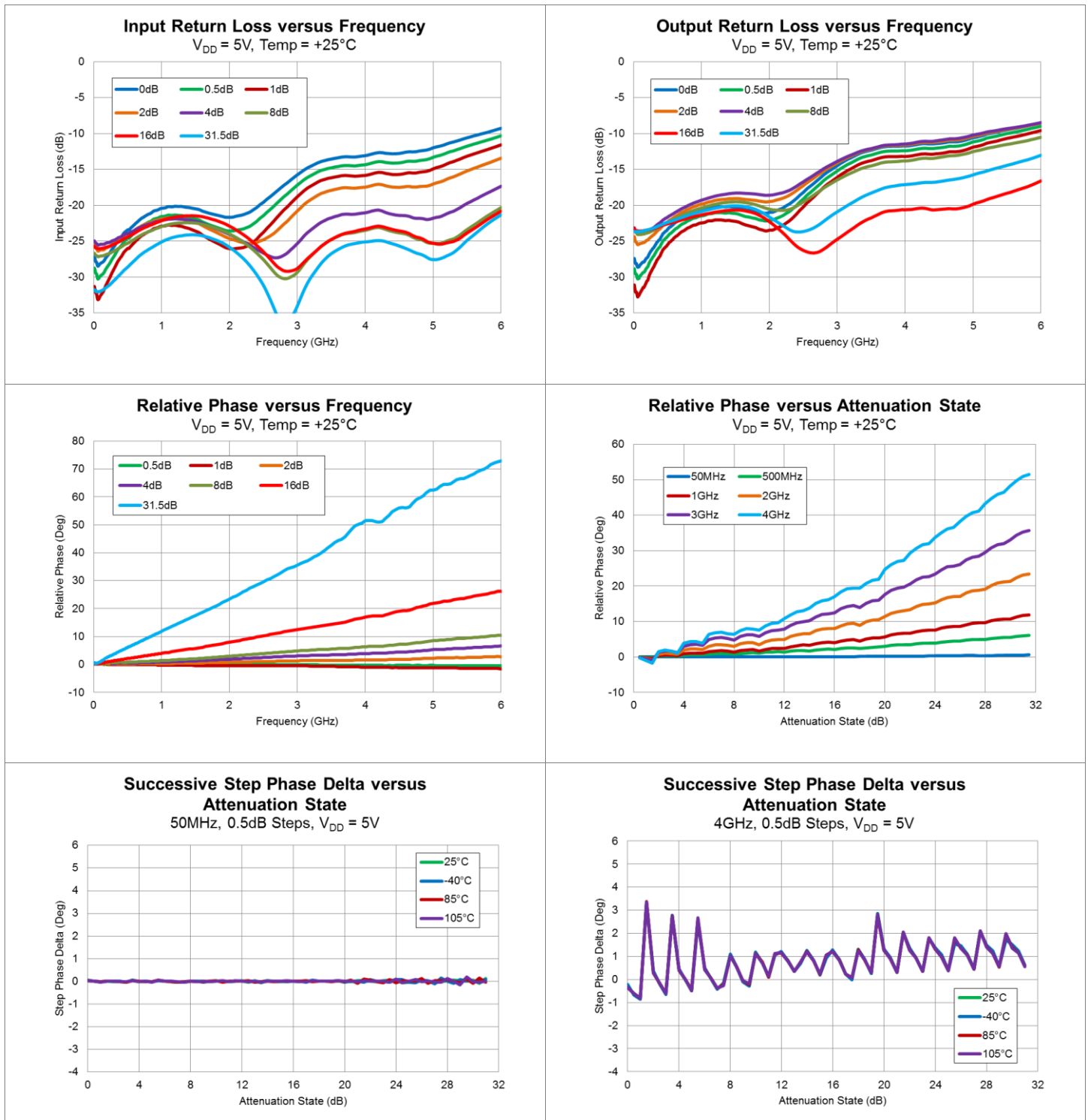


## 12. Typical Performance Plots (2)

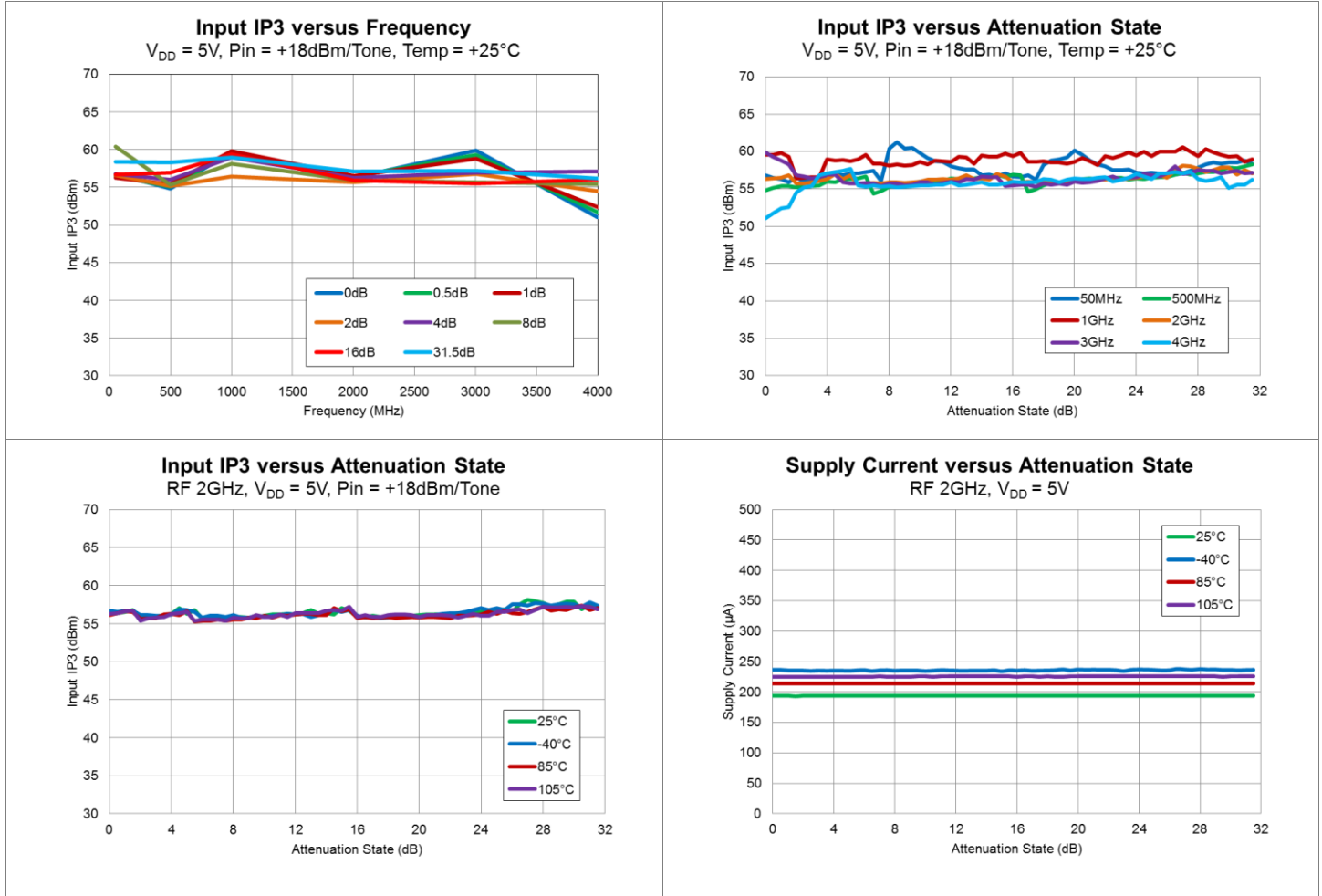


DSA control remains monotonic if step error is within  $\pm 0.5dB$

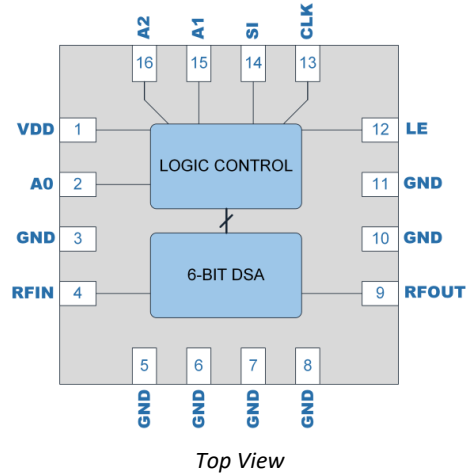
### 13. Typical Performance Plots (3)



### 14. Typical Performance Plots (4)



## 15. Pin Configuration and Description

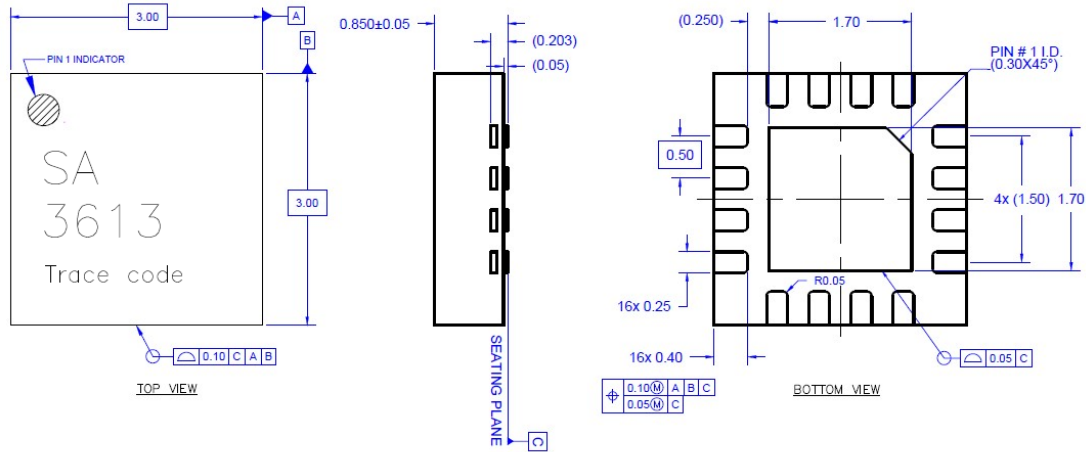


Pin Number	Label	Description
1	VDD	DC Supply Voltage Input
2	A0	External Address bit-0 Pin
3, 5, 6, 7, 8, 10, 11	GND	RF and DC Ground Pin
4	RFIN	RF Input Pin, Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply non-Zero DC voltage to this pin. Internally the ground returns thru resistors. Additional external DC ground return allowed
9	RFOUT	RF Output Pin. Do not apply non-Zero DC voltage to this pin. Internally the ground returns thru resistors. Additional external DC ground return allowed
12	LE	Latch Enable Pin. The raising edge of it triggering the attenuator to change state
13	CLK	Serial Clock Input Pin
14	SI	Serial data Input Pin
15	A1	External Address bit-1 Pin
16	A2	External Address bit-2 Pin
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB via holes under the device are required.

## 16. Packaging and Ordering Information

### 16.1. Device Marking and Package Dimensions

Marking: Part number — SA3613  
Trace code — Assigned by Sub-contractor



**Notes:**

1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012

## 17. Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA/JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020



**Caution!**

ESD sensitive device

## 18. Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Matte Sn (*Plating thickness: 8 to 23µm*)

## 19. Environmental Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- SVHC Free
- PFOS Free



## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Tel:** +1 844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

## Important Notices

The information contained in this Data Sheet and any associated documents ("Data Sheet Information") is believed to be reliable; however, Qorvo makes no warranties regarding the Data Sheet Information and assumes no responsibility or liability whatsoever for the use of or reliance on said information. All Data Sheet Information is subject to change without notice. Customers should obtain and verify the latest relevant Data Sheet Information before placing orders for Qorvo® products. Information concerning Qorvo's product life cycles is available at <https://www.qorvo.com/support/product-lifecycle-information>. Data Sheet Information or the use thereof does not grant, explicitly, implicitly or otherwise any rights or licenses with respect to patents or any other intellectual property whether with regard to such Data Sheet Information itself or anything described by such information.

Qorvo grants you permission to use this Data Sheet and any associated resources only to develop an application that uses the Qorvo products described in the Data Sheet and any associated resources. Other reproduction and display of this Data Sheet and any associated resources is prohibited.

Qorvo's products are provided subject to Qorvo's [Terms of Sale](#) or provided in conjunction with such Qorvo products. Qorvo objects to and rejects any additional or different terms customer may have proposed regarding the purchase of Qorvo products.

DATA SHEET INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. Applications described in the Data Sheet Information are for illustrative purposes only. Customers are responsible for validating that a particular product described in the Data Sheet Information is suitable for use in a particular application.

© 2026 Qorvo US, Inc. All rights reserved. This document is subject to copyright laws in various jurisdictions worldwide and may not be reproduced or distributed, in whole or in part, without the express written consent of Qorvo US, Inc.

QORVO® is a registered trademark of Qorvo US, Inc. All other trademarks and trade names are property of their respective owners.